Germanane MOSFET for Subdeca Nanometer High-Performance Technology Nodes

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***Abstract*— Ballistic transport in monolayer Germanane MOSFETs is investigated for high-performance (HP) applications. Characteristics of both n- and p-type transistors having channel lengths of 7, 5, and 3 nm are studied and compared against the International Technology Roadmap for Semiconductor (ITRS) target of 2028. Our simulation approach is based on a self-consistent quantum ballistic transport model within the framework of the nonequilibrium Green's function formalism and relies on a single-band and a two-band $k \cdot p$ Hamiltonian for n- and p-type channels, respectively. We found that, even for a gate length scaled down to 3 nm, the ON current (I_{ON}) in n- and p-MOSFETs for a fixed OFF current I_{OFF} = 100 nA/μm is as high as ~890 and 700 μA/μm, respectively. For longer channel lengths, the p-MOSFET can outperform the n-MOSFET in terms of I_{ON} requirements, as the direct source-to-drain tunneling gets suppressed. Other performance metrics, including gate capacitance, intrinsic switching delay, and switching energy, have also been calculated and found to be comparable to the ITRS 2028 HP technology requirements.**

***Index Terms*— 2-D materials, ballistic transport, Germanane, International Technology Roadmap for Semiconductor (ITRS), nonequilibrium Green's function (NEGF) formalism.**

I. Introduction

IN RECENT times, atomically thin 2-D materials are being extensively explored as an alternative channel material for transistor technologies able to meet Moore's law projections in the long-term future. Most of these materials, e.g., graphene, hBN, phosphorene, transition metal dichalcogenides (TMD), such as MoS_2, WS_2, $MoSe_2$, WSe_2, $MoTe_2$, and so on [1]–[9], are naturally available in layered form, where 2-D platelets are weakly bonded by van der Waals forces to form 3-D crystals. In an alternate route, recent efforts are also observed to extract 2-D analogues from conventional bulk semiconductors, such as Si, Ge, and GaN [10]–[15]. Among these materials, germanane, a hydrogenated monolayer of germanium, has attracted much attention. Unlike TMDs, which show higher bandgap and higher effective mass, Germanane inherits a very interesting property of having low effective mass along with a relatively high bandgap [15]. From recent first principle-based assessments [16], it was further concluded that chair morphology of Germanane has better potential for conventional and tunnel FET applications than its boat morphology. Stable structure of Germanane has been reported for the first time in 2013 [15], and later used for fabrication of Schottky diodes and FETs [17]–[19].

Since high-performance (HP) switching devices demand channel materials with low effective mass to ensure high ON current, Germanane stands a very good chance in this respect. It is therefore important to theoretically estimate the performance limit of Germanane channel MOSFETs. However, previous studies of such devices are either based on a semiclassical approach [20] or limited only to the n-MOSFETs [21]. In this paper, we focus on nonequilibrium Green's function (NEGF) simulations of ballistic transport in both n- and p-type Germanane chair MOSFETs with channel lengths less than 10 nm, to assess if such short channel Germanane MOSFETs are able to meet the International Technology Roadmap for Semiconductor (ITRS) 2028 HP (2013 edition) projections [22].

This paper is organized as follows. In Section II, we describe the simulation methodology. In Section III, we present and discuss our results in relation to the device static and dynamic figures of merits. A benchmark of the performance of the considered devices against other reported 2-D-material-based MOSFETs is also proposed. Finally, in Section IV, we draw our concluding remarks.

II. Methodology

A sketch of the simulated device cross section is shown in Fig. 1. We set the device parameter so as to be close to the ITRS-predicted physical gate length, effective oxide

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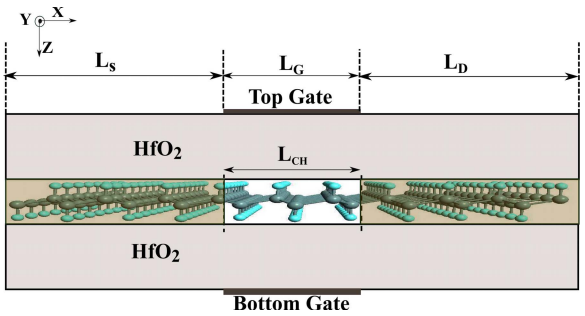

Fig. 1. Sketch of the cross section of the considered Germanane-chair-based MOSFET. L_{CH} denotes the channel length, which equals the gate length L_G. The channel is undoped, whereas the source and drain extensions (shaded) are uniformly doped.

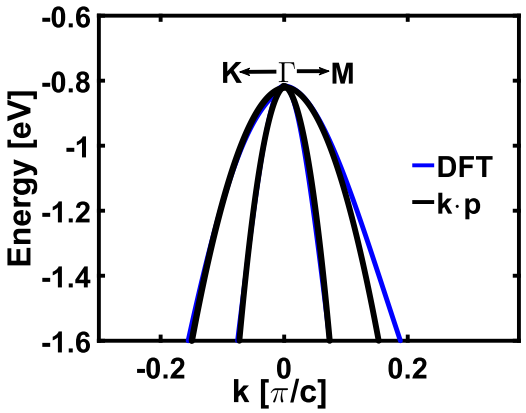

Fig. 2. Germanane chair valence-band structure close to the Γ point compared with the two-band $k \cdot p$ model. $c = 0.393$ nm.

thickness (EOT), and power supply voltage for the 2028 HP devices. The length L_{CH} of the undoped channel is the same as the gate length L_G. In order to investigate the scaling behavior of the devices, three different values, 7, 5, and 3 nm, have been considered for L_{CH}. EOT is set to 0.47 nm. The supply bias is V_D= 0.6 V. The source and drain extensions are uniformly doped. Their length (L_S and L_D, respectively) is set to 30 nm, in order to ensure the charge neutrality at the contacts. The thickness of the Germanane layer is taken to be 0.37 nm, as extracted from the relaxed atomic structure reported in [16]. The gate work-function is adjusted so that the OFF-state current (I_{OFF}) at zero gate voltage (V_G) is set at 100 nA/μm for all the devices under study.

Monolayer Germanane in the chair configuration has isotropic conduction band and valence bands (light hole and heavy hole) [16]. Therefore, for n-MOSFET, we have chosen a single band effective mass Hamiltonian with electron effective mass of $0.071m_o$ [16]. For the p-MOSFET, we developed a two-band $k \cdot p$ Hamiltonian based on its analogous Graphane counterpart [23] and given as

$$H(\mathbf{k}) \equiv \begin{bmatrix} \frac{\gamma_1}{2}\left(k_x{}^2 + k_y{}^2\right) & \frac{\gamma_2}{2}(k_x + ik_y)^2 \\ \frac{\gamma_2}{2}(k_x - ik_y)^2 & \frac{\gamma_1}{2}\left(k_x{}^2 + k_y{}^2\right) \end{bmatrix}, \tag{1}$$

where $\mathbf{k} = (k_x, k_y)$ is the in-plane wave vector and

$$\begin{aligned} \gamma_1 &= \frac{1}{2}\left(\frac{1}{m_L} + \frac{1}{m_H}\right) \\ \gamma_2 &= \frac{1}{2}\left(\frac{1}{m_L} - \frac{1}{m_H}\right) \end{aligned} \tag{2}$$

where m_{L} and m_{H} are the light hole and heavy hole effective masses, respectively. By assuming m_{L} and m_{H} equal $0.071m_o$ and $0.29m_o$, respectively [16], the $k \cdot p$ band structure is found to be in good agreement with the density functional theory predictions [16] in a window of ~ 0.3 eV close to the valence band maximum at the Γ point of the Brillouin zone (see Fig. 2).

The doping concentrations in the source and drain extensions have been chosen for each device so as to maximize the I_{ON}/I_{OFF} ratio. For L_{CH} equal to 3, 5, and 7 nm, the optimum doping concentration turns out to be 3.5×10^{12}, 3.5×10^{12}, and $3.9 \times 10^{12}/\mathrm{cm}^2$, respectively, for n-MOSFETs, and 4.8×10^{12}, 5.2×10^{12}, and $5.2 \times 10^{12}/\mathrm{cm}^2$, respectively, for p-MOSFETs. We found that doping concentrations lower than $10^{12}/\mathrm{cm}^2$ result in source exhaustion [24], whereas concentrations higher than $10^{13}/\mathrm{cm}^2$ strongly degrade the subthreshold swing. We model the transport by self-consistently solving the transport equations within the Keldysh formalism [25] and the Poisson equation. The device is assumed translationally invariant in the y-direction, which entails that the Hamiltonian and the Green's functions can be parameterized in terms of the transversal wave vector k_y and that we can restrict the solution of the Poisson equation to a cross section in the xz plane. We included in our computation 20 uniformly spaced transversal wave vectors $k_{y,n} = 2\pi n/L_y$, chosen to fulfill the Born-von Karman periodic boundary conditions in a system with finite length $L_y = 150$ nm. For each wave vector k_y, the retarded Green's function (expressed in the matrix notation) is calculated as [26], [27]

$$G^r(k_y, E) = [EI - H(k_y) - \Sigma_S - \Sigma_D]^{-1} \tag{3}$$

where E is the energy, $H(k_y)$ is the Hamiltonian matrix discretized along the transport direction x, I is the identity matrix, and Σ_S/Σ_D are self-energy matrices associated with the source/drain contacts [26]. From the retarded Green's function $G^r(k_y, E)$, we calculate the electron and hole Green's functions $G^n(k_y, E)$ and $G^p(k_y, E)$ as follows:

$$\begin{aligned} G^n(k_y, E) &= G^r(k_y, E)\Sigma_n G^{r\dagger}(k_y, E) \\ G^p(k_y, E) &= G^r(k_y, E)\Sigma_p G^{r\dagger}(k_y, E) \end{aligned} \tag{4}$$

where

$$\begin{aligned} \Sigma_n &\equiv \left(\Sigma_{S/D} - \Sigma_{S/D}{}^{\dagger}\right) \cdot f_{S/D} \\ \Sigma_p &\equiv \left(\Sigma_{S/D} - \Sigma_{S/D}{}^{\dagger}\right) \cdot (1 - f_{S/D}) \end{aligned} \tag{5}$$

with † denoting the transpose conjugate and $f_{S/D}$ denoting the Fermi–Dirac distribution function at source/drain. The carrier densities are calculated from the ith diagonal elements of

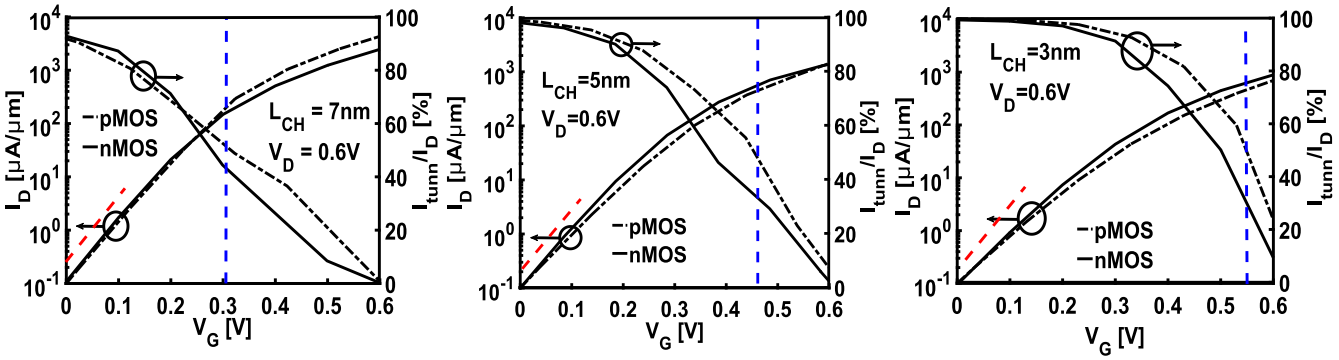

Fig. 3. Transfer characteristics and percentage of tunneling current in Germanane MOSFETs for (a) L_{CH} = 7 nm, (b) L_{CH} = 5 nm, and (c) L_{CH} = 3 nm and for a drain bias of V_D= 0.6 V. The vertical blue dashed line indicates the gate voltage at which the percentage of tunneling current in p-MOSFET is 50%. The red dotted line represents the slope at V_G= 0 of the transfer characteristic of the n-MOSFET with L_{CH} = 7 nm. It is marked on all the panels as reference. The tunneling current I_{tunn} is computed by integrating the current spectrum in the energy window between the smallest (highest) energy considered in the simulation and the energy corresponding to the top of the barrier for electrons (holes).

$G^n(k_y, E)$ and $G^p(k_y, E)$ as

$$n_i = \sum_{k_y} \frac{1}{S} \int_{-\infty}^{+\infty} \frac{G^n{}_{ii}(k_y, E)}{2\pi} dE$$
$$p_i = \sum_{k_y} \frac{1}{S} \int_{-\infty}^{+\infty} \frac{G^p{}_{ii}(k_y, E)}{2\pi} dE \quad (6)$$

and the current density flowing from position i to $i+1$ along the x-direction is calculated from the off-diagonal elements $(i, i+1)$ of $G^{n(p)}(k_y, E)$ as

$$J^{n(p)}{}_{i,i+1} = \sum_{k_y} \frac{2q}{\hbar S} \int_{-\infty}^{+\infty} \frac{dE}{2\pi} [H_{i,i+1} G^{n(p)}{}_{i+1,i}(k_y, E) - H_{i+1,i} G^{n(p)}{}_{i,i+1}(k_y, E)] \quad (7)$$

where $H_{i,i+1}$ corresponds to the nearest neighbor hopping terms in the discretized Hamiltonian. In (6) and (7), $S = L_y \times \Delta x$, where Δx is the discretization step in the x-direction. The carrier and current density are computed by the recursive Green's function algorithm [28], [29]. For discretizing the 2-D Poisson equation in the cross section of the device, we use the finite difference method, enforcing Dirichlet boundary conditions at the metal gate electrodes and Neumann boundary conditions on the rest of the edges. The NEGF transport equations and the Poisson equation are solved iteratively until self-consistency is achieved. Mixed C and MATLAB [30] programming style is used to speed up the recursive Green's function algorithm [31]. Parallel computation for the transverse modes resulted in a further reduction of the computational time.

In the following part of this section, we will discuss in detail some of the approximations contained in our model.

In this paper, ballistic transport is assumed. In order to assess the validity of this approximation, we have estimated the phonon-limited mean-free path of carriers as $\lambda = v_F \times \tau_{ph}$, where v_F is the injection Fermi velocity at source and τ_{ph} is the average time between phonon-scattering events. For n-MOSFETs, $v_F \sim 8 \times 10^7$ cm/s and τ_{ph} can be calculated from the value of mobility reported in [15]. We obtain $\lambda_e \approx 590$ nm. Concerning holes, no estimates of mobility in Germanane are available in the literature. If, as a rough approximation, we assume for holes the same τ_{ph} calculated for electrons, we obtain, $\lambda_{lh} \approx 250$ nm ($v_F \sim 4 \times 10^7$ cm/s) and $\lambda_{hh} \approx 150$ nm ($v_F \sim 2 \times 10^7$ cm/s), for light holes and heavy holes, respectively. All these estimates for the mean-free path largely exceed the channel lengths considered in this paper, therefore suggesting that for these devices, the carrier-phonon interaction is actually negligible.

Another aspect to consider concerns the parasitics. Our simulations do not take into account the parasitic source and drain resistances, as the rapid evolution of the contact fabrication techniques in 2-D materials makes it difficult to reliably predict their future values. Moreover, the simplified geometry modeling of our devices cannot take into account the fringe field associated with the gate sidewalls and the source and drain contact plugs and therefore results in an underestimation of the parasitic capacitances. In most of the cases, these approximations will result in estimates of the device figures of merit optimistically close to the upper limit of the achievable performance. On the other hand, this approach makes our results directly comparable with those already published in similar studies [35], [36], which are routinely obtained within the same approximations.

III. Results and Discussion

We first investigate the static I_D–V_G characteristics of monolayer Germanane MOSFETs followed by the dynamic performance metrics. Transfer characteristics of both n- and p-MOSFETs have been examined and the simulated I_D–V_G plots for various channel lengths are shown in Fig. 3. I_{ON} in monolayer Germanane n-MOSFETs for L_{CH} = 7, 5, and 3 nm are 2.5, 1.7, and 0.89 mA/μm, respectively, whereas those for p-MOSFETs are 4.32, 1.44, and 0.7 mA/μm, respectively, as reported in Table I. According to these results, the Germanane-based devices with channel length scaled to the remarkably small dimension of 3 nm still appear to be able to provide an ON-current comparable to the ITRS projected value.

TABLE I
PERFORMANCE METRICS COMPARISON OF GERMANANE MONOLAYER MOSFETS WITH ITRS 2028 PREDICTION

Parameter	Germanane nMOS			Germanane pMOS			2028 HP FET
L_{CH} (nm)	7	5	3	7	5	3	4.1
I_{ON}(mA/μm)	2.50	1.7	0.89	4.32	1.44	0.70	0.90
C_G (fF/μm)	0.22	0.16	0.12	0.90	0.51	0.14	0.60
τ (fs)	39	57	72	47	69	107	423
PDP (aJ/μm)	58	47	38	118	82	45	600

The gradual decrease of I_{ON} as the channel length is scaled down can be explained by considering the concomitant increase of the source-to-drain tunneling. Due to the enhancement of the tunneling, shorter devices require a higher barrier in the OFF state in order to ensure the same I_{OFF} of devices with longer channels. A higher barrier in the OFF state directly entails a higher barrier in the ON state, resulting in a degradation of I_{ON}. The enhancement of the tunneling for decreasing L_{CH} also results in the degradation of the slope of the transfer characteristics at low V_G (see Fig. 3) which further contributes to the I_{ON} reduction.

The transfer characteristics in Fig. 3 also allow us to compare the behavior of n- and p-MOSFETs, both as a function of V_G and L_{CH}. We focus first on the low-V_G region. The slope of the transfer characteristics is found to be always higher in the case of n-MOSFETs. This difference can be explained by contrasting the position of the source Fermi level (E_{FS}) with respect to the transport-band edge in p-MOSFETs and n-MOSFETs. While the doping concentration in p- and n-MOSFETs is very close, in the former, the density of states (DOS) is substantially higher than that in the latter due to the contribution of the heavy hole subband. As a consequence, the charge neutrality condition at the source contact enforces a smaller distance of E_{FS} from the valence band edge in p-devices than between E_{FS} and the conduction band edge in n-devices. This translates to a different distribution of the carrier injection energies (see the current spectra in Fig. 4). In p-MOSFETs, carriers are injected close to the base of the channel barrier and forced to tunnel. On the contrary, in n-MOSFETs, E_{FS} is far enough from the conduction band edge to allow a substantially higher thermionic component to flow. The higher tunneling in p-MOSFETs degrades the electrostatic control over the current, resulting in a lower slope. The n-MOSFET and p-MOSFET transfer characteristics in the low V_G regime get close as the channel length increases, due to a reduction of the relative importance of the tunneling.

The scenario changes for high V_G. By closely observing the plots in Fig. 3, we notice that when the percentage of tunneling current decreases below $\sim$ 50%, the current in p-MOSFETs starts rising faster than in n-MOSFETs. The approximate V_G value, $V_{50\%}$, at which this effect starts arising depends on the channel length and increases as L_{CH} decreases. For $V_{50\%}$ close to V_D (L_{CH} = 5 and 3 nm), the I_{ON} in p-MOSFETs can only get closer to the one of n-MOSFETs, while it can exceed it for low enough $V_{50\%}$ (L_{CH} = 7 nm). This behavior originates from the filtering effect of the channel barrier, which allows light holes to tunnel, while blocking the heavy holes due to the bigger effective mass. The heavy holes mainly contribute to the transport by sustaining the thermionic current, which starts to play a significant role when the channel barrier is low enough. This threshold condition is approximately realized for $V_G \approx V_{50\%}$, since for higher gate voltages, the percentage contribution of the thermionic current exceeds that of the tunneling current. As previously discussed, for a given V_G, longer devices exhibit a smaller barrier with respect to the shorter ones. This explains the dependence of $V_{50\%}$ on L_{CH} and in turn, of the difference of I_{ON} between n- and p-MOSFETs.

We discuss now the dynamic performance of the devices, quantified in terms of intrinsic switching delay (τ), gate capacitance (C_G), and power delay product (PDP). All the values are listed in Table I. The intrinsic switching delay is computed following the method explained in [32] as $\tau = (Q_{ON} - Q_{OFF})/I_{ON}$, where Q_{ON} and Q_{OFF} are the overall charges induced in the device at the ON-state and OFF-state, respectively. The gate capacitance is calculated by differentiating the total charge along the entire length of the device with respect to the gate voltage as $C_G = \partial Q/\partial V_{GS}$. The PDP is calculated as $V_D(Q_{ON} - Q_{OFF})$ [33]. In Fig. 5, we plot C_G as a function of V_G and for different L_{CH} values. Significant deviations in the behavior of C_G in n- and p-MOSFETs arise for large enough gate voltages. The sudden increase of C_G in p-MOSFETs reflects the increase of the quantum capacitance $C_Q \propto \mathrm{DOS}(E_{FS})$ [26], when the top of barrier gets lower than E_{FS}. The effect is much lower in n-MOSFETs, for which C_Q is limited by the low DOS. For both n- and p-MOSFETs, the values of τ and PDP (see Table I), which basically express the upper limit performance as mentioned in Section II, are substantially lower than the ITRS requirements (up to one order of magnitude for the n-MOSFET with L_{CH} = 7 nm). As a function of L_{CH}, we find for τ and PDP opposite trends: τ increases as L_{CH} is scaled down, while PDP decreases. The behavior of PDP is due to the decrease of C_G when L_{CH} is reduced (see Fig. 5), which entails a reduction of Q_{ON}–$Q_{OFF} = \int_0^{V_D} C_G\, dV_G$. The increase of τ reflects the strong enhancement of the tunneling for short L_{CH}, which entails that I_{ON} decreases faster than (Q_{ON}–Q_{OFF}) when L_{CH} is scaled down. According to this analysis, the worse performance of p-MOSFETs with respect to n-MOSFETs in terms of PDP and τ derive from the bigger gate capacitance and the higher percentage of tunneling, respectively.

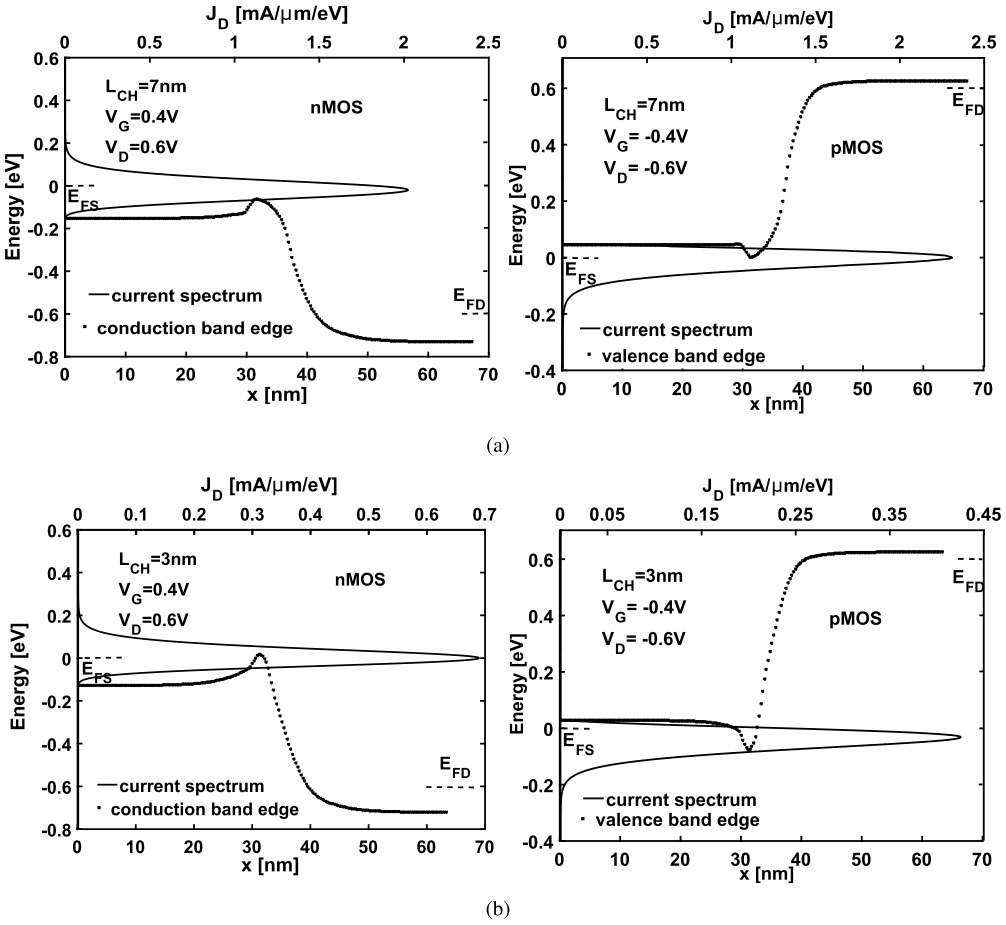

Fig. 4. Energy resolved current spectrum superimposed on the conduction (valence) band edge profile for Germanane n-MOSFET (p-MOSFET) with (a) $L_{CH} = 7$ nm and (b) $L_{CH} = 3$ nm.

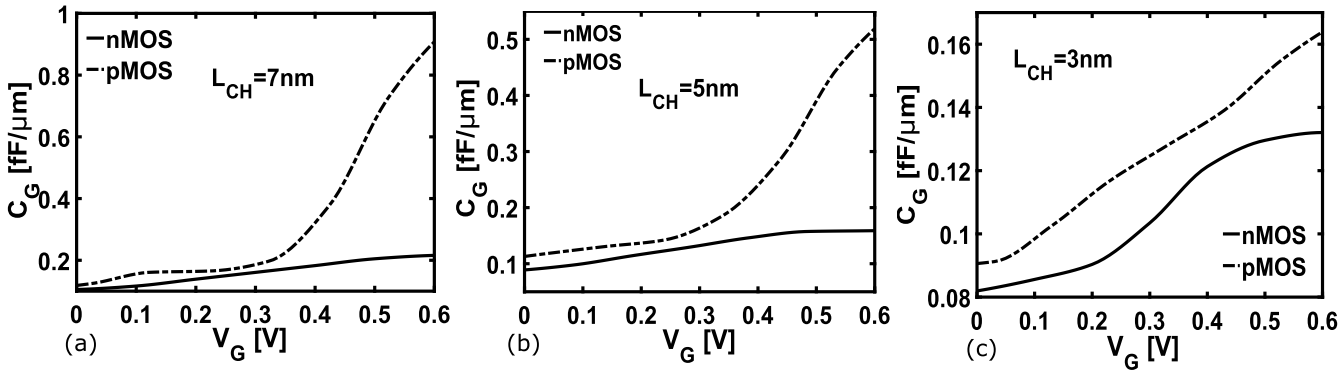

Fig. 5. Gate capacitance as a function of the gate bias for Germanane MOSFETS with (a) $L_{CH} = 7$ nm, (b) $L_{CH} = 5$ nm, and (c) $L_{CH} = 3$ nm.

Finally, we compare the energy efficiency and the switching capability of Germanane monolayer (GeH) MOSFETs with respect to other 2-D material-based MOSFETs, namely monolayer black phosphorus (BP) MOSFETs in Armchair (A) and Zigzag (Z) directions and MoS2 MOSFETs for two different channel lengths. For these devices, we plot in Figs. 6 and 7 PDP versus τ and τ versus I_{ON}/I_{OFF}, respectively. In Figs. 6 and 7, it can been seen that Germanane MOSFETs can largely meet the ITRS HP as well as III-V/Ge HP FET requirements. Fig. 6 shows that the points referring to the most performant devices, namely Germanane n-MOSFETs, BP MOSFETs, and the MoS_2 MOSFET with the shorter channel, gather around the equi-(PDP·τ) curve with PDP·$\tau \approx 3 \times 10^{-30}$ Js/μm. This expresses the common PDP-τ tradeoff, according to which the switching speed can be increased at the expense of a higher energy consumption. Among the above-mentioned devices, the Armchair BP MOSFET exhibits the smaller intrinsic switching delay, while the Germanane n-MOSFET with $L_{CH} = 3$ nm exhibits the lowest switching energy. Fig. 7 highlights that the Germanane

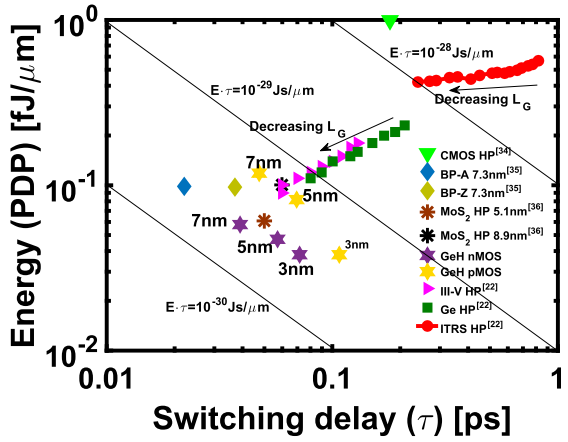

Fig. 6. Performance benchmark in the PDP-τ plane against other reported 2-D materials MOSFETs. GeH denotes the Germanane MOSFETs; CMOS HP denotes the 15-nm technology node at V_D = 0.73 V; BP-A and -Z denote HP monolayer BP MOSFETs in Armchair and Zigzag directions, respectively, with $L_{\rm CH} = 7.3$ nm and $V_D = 0.69$ V; MoS_2 HP denotes Molybdenum disulfide MOSFETs with $L_{\rm CH} = 5.1$ and 8.3 nm at $V_D = 0.5$ V. The ITRS predicted trend lines until the end of the roadmap for silicon as well as for III-V/Ge HP technologies are also shown in the map for reference. The straight lines are the equi-(PDP·τ) curves.

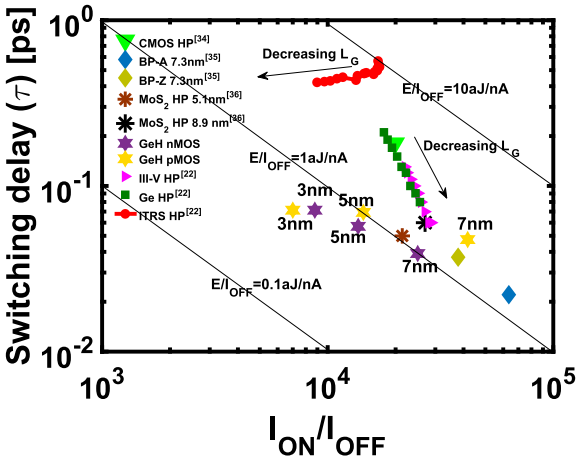

Fig. 7. Performance benchmark in the τ-$I_{\rm ON}/I_{\rm OFF}$ plane against other reported 2-D materials MOSFETs. The straight lines are the equi-(PDP/$I_{\rm OFF}$) curves.

n- and p-MOSFETs with $L_{\rm CH} = 7$ nm, the MoS_2 MOSFETs, and the Zigzag BP MOSFET belong to a quite restricted region of the τ-$I_{\rm ON}/I_{\rm OFF}$ plane, with a dispersion in τ of $\sim 3 \times 10^{-2}$ ps and 2×10^4 in the $I_{\rm ON}/I_{\rm OFF}$ ratio. Only the Armchair BP MOSFET exhibits better performance.

IV. Conclusion

We investigated through self-consistent full quantum simulations the potentialities of sub-10-nm gate-length Germanane MOSFETs against the ITRS 2028 projections for HP devices. We found that both Germanane n-MOSFET and p-MOSFET offer excellent $I_{\rm ON}$ and large $I_{\rm ON}/I_{\rm OFF}$ ratios even when scaled down to 3-nm channel length, which is beyond the ITRS projected limits. The values obtained for the dynamic figure of merit, such as intrinsic switching delay and PDP, indicate that both n- and p-MOSFETs could meet the ITRS projections and compete with other 2-D material-based MOSFETs. This paper therefore suggests that Germanane MOSFETs represent a viable option for HP ultrascaled device applications.

References

[1] B. Radisavljevic, M. B. Whitwick, and A. Kis, "Integrated circuits and logic operations based on single-layer MoS_2," *ACS Nano*, vol. 5, no. 12, pp. 9934–9938, Nov. 2011, doi: 10.1021/nn203715c.

[2] S. B. Desai *et al.*, "MoS_2 transistors with 1-nanometer gate lengths," *Science*, vol. 354, no. 6308, pp. 99–102, Oct. 2016, doi: 10.1126/science.aah4698.

[3] H. Fang, S. Chuang, T. C. Chang, K. Takei, T. Takahashi, and A. Javey, "High-performance single layered WSe_2 p-FETs with chemically doped contacts," *Nano Lett.*, vol. 12, no. 7, pp. 3788–3792, Jun. 2012, doi: 10.1021/nl301702r.

[4] L. Liu, S. B. Kumar, Y. Ouyang, and J. Guo, "Performance limits of monolayer transition metal dichalcogenide transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 3042–3047, Sep. 2011, doi: 10.1109/TED.2011.2159221.

[5] R. K. Ghosh and S. Mahapatra, "Monolayer transition metal dichalcogenide channel-based tunnel transistor," *IEEE J. Electron Devices Soc.*, vol. 1, no. 10, pp. 175–180, Oct. 2013, doi: 10.1109/TED.2011.2159221.

[6] L. Li *et al.*, "Black phosphorus field-effect transistors," *Nature Nanotech.*, vol. 9, no. 5, pp. 372–377, May 2014, doi: 10.1038/nnano.2014.35.

[7] H. Liu *et al.*, "Phosphorene: An unexplored 2D semiconductor with a high hole mobility," *ACS Nano*, vol. 8, no. 4, pp. 4033–4041, Mar. 2014, doi: 10.1021/nn501226z.

[8] D. Golberg *et al.*, "Boron nitride nanotubes and nanosheets," *ACS Nano*, vol. 4, no. 6, pp. 2979–2993, May 2010, doi: 10.1021/nn1006495.

[9] K. S. Novoselov *et al.*, "Two-dimensional atomic crystals," *Proc. Nat. Acad. Sci. USA*, vol. 102, no. 30, pp. 10451–10453, Jul. 2005, doi: 10.1073/pnas.0502848102.

[10] K. J. Koski and Y. Cui, "The new skinny in two-dimensional nanomaterials," *ACS Nano*, vol. 7, no. 5, pp. 3739–3743, May 2013, doi: 10.1021/nn4022422.

[11] Z. Y. Al Balushi *et al.*, "Two-dimensional gallium nitride realized via graphene encapsulation," *Nature Mater.*, vol. 15, no. 11, pp. 1166–1171, Nov. 2016, doi: 10.1038/nmat4742.

[12] L. C. L. Yan Voon, E. Sandberg, R. S. Aga, and A. A. Farajian, "Hydrogen compounds of group-IV nanosheets," *Appl. Phys. Lett.*, vol. 97, no. 16, pp. 163114-1–163114-3, Oct. 2010, doi: 10.1063/1.3495786.

[13] J. C. Garcia, D. B. de Lima, L. V. C. Assali, and J. F. Justo, "Group IV Graphene- and Graphane-Like Nanosheets," *J. Phys. Chem. C*, vol. 115, no. 27, pp. 13242–13246, Jun. 2011, doi: 10.1021/jp203657w.

[14] O. Pulci, P. Gori, M. Marsili, V. Garbuio, R. D. Sole, and F. Bechstedt, "Strong excitons in novel two-dimensional crystals: Silicane and Germanane," *Europhys. Lett.*, vol. 98, no. 3, pp. 37004-p1–37004-p5, May 2012, doi: 10.1209/0295-5075/98/37004.

[15] E. Bianco, S. Butler, S. Jiang, O. D. Restrepo, W. Windl, and J. E. Goldberger, "Stability and exfoliation of Germanane: A germanium graphane analogue," *ACS Nano*, vol. 7, no. 5, pp. 4414–4421, Mar. 2013, doi: 10.1021/nn4009406.

[16] R. K. Ghosh, M. Brahma, and S. Mahapatra, "Germanane: A low effective mass and high bandgap 2-D channel material for future FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2309–2315, Jul. 2014, doi: 10.1109/TED.2014.2325136.

[17] W. Amamou *et al.*, "Large area epitaxial Germanane for electronic devices," *2D Mater.*, vol. 2, no. 3, pp. 035012-1–035012-8, Aug. 2015, doi: 10.1088/2053-1583/2/3/035012.

[18] B. N. Madhushankar *et al.*, "Electronic properties of Germanane field-effect transistors," *2D Mater.*, vol. 4, no. 2, pp. 021009-1–021009-6, Feb. 2017, doi: 10.1088/2053-1583/aa57fd.

[19] N. G. Sahoo, R. J. Esteves, V. D. Punetha, D. Pestov, I. U. Arachchige, and J. T. McLeskey, Jr., "Schottky diodes from 2D Germanane," *Appl. Phys. Lett.*, vol. 109, no. 2, pp. 023507-1–023507-4, Jul. 2016, doi: 10.1063/1.4955463.

[20] K. L. Low, W. Huang, Y.-C. Yeo, and G. Liang, "Ballistic transport performance of silicane and Germanane transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 5, pp. 1590–1598, May 2014, doi: 10.1109/TED.2014.2313065.

[21] A. AlMutairi, Y. Zhao, D. Yin, and Y. Yoon, "Performance limit projection of Germanane field-effect transistors," *IEEE Electron Device Lett.*, vol. 38, no. 5, pp. 673–676, May 2017, doi: 10.1109/LED.2017.2681579.

[22] *International Technology Roadmap for Semiconductors*. Accessed: Nov. 25, 2017. [Online]. Available: http://www.itrs2.net/2013-itrs.html
[23] I. V. Tokatly, "Orbital momentum Hall effect in *p*-doped graphane," *Phys. Rev. B, Condens. Matter*, vol. 82, no. 16, pp. 161404-1–161404-4, Oct. 2010, doi: 10.1103/PhysRevB.82.161404.
[24] R. Kim, U. E. Avci, and I. A. Young, "Source/drain doping effects and performance analysis of ballistic III–V n-MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 3, no. 1, pp. 37–43, Jan. 2015, doi: 10.1109/JEDS.2014.2363389.
[25] G. Stefanucci and R. V. Leeuwen, *Nonequilibrium Many-Body Theory of Quantum Systems: A Modern Introduction*. Cambridge, U.K.: Cambridge Univ. Press, 2013, doi: 10.1017/CBO9781139023979.
[26] S. Datta, *Quantum Transport: Atom to Transistor*. Cambridge, U.K.: Cambridge Univ. Press, 2005, doi: 10.1017/CBO9781139164313.
[27] J. Guo, "Carbon nanotube electronics: Modeling, physics, and applications," Ph.D. dissertation, Dept. Elect. Eng., Purdue Univ., West Lafayette, IN, USA, Aug. 2004. [Online]. Available: https://nanohub.org/resources/1928
[28] R. Lake, G. Klimeck, R. C. Bowen, and D. Jovanovic, "Single and multiband modeling of quantum electron transport through layered semiconductor devices," *J. Appl. Phys.*, vol. 81, no. 12, pp. 7845–7869, Jun. 1997, doi: 10.1063/1.365394.
[29] M. P. Anantram, M. S. Lundstrom, and D. E. Nikonov, "Modeling of Nanoscale Devices," *Proc. IEEE*, vol. 96, no. 9, pp. 1511–1550, Sep. 2008, doi: 10.1109/JPROC.2008.927355.
[30] *MATLAB Version 9.1.0.441655 (R2016b)*, MathWorks, Inc., Natick, MA, USA, Sep. 2016.
[31] Z. Jiang, "Quantum transport in RTD and atomistic modeling of nanostructures," M.S. thesis, Dept. Elect. Eng., Purdue Univ., West Lafayette, IN, USA, 2011.
[32] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Performance comparison between pin tunneling transistors and conventional MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 3, pp. 456–465, Mar. 2009, doi: 10.1109/TED.2008.2011934.
[33] D. Logoteta, G. Fiori, and G. Iannaccone, "Graphene-based lateral heterostructure transistors exhibit better intrinsic performance than graphene-based vertical transistors as post-CMOS devices," *Sci. Rep.*, vol. 4, no. 1, Oct. 2014, Art. no. 6607, doi: 10.1038/srep06607.
[34] K. Majumdar, C. Hobbs, and P. D. Kirsch, "Benchmarking transition metal dichalcogenide MOSFET in the ultimate physical scaling limit," *IEEE Electron Device Lett.*, vol. 35, no. 3, pp. 402–404, Mar. 2014, doi: 10.1109/LED.2014.2300013.
[35] F. Liu, Y. Wang, X. Liu, J. Wang, and H. Guo, "Ballistic transport in monolayer black phosphorus transistors," *IEEE Trans. Electron Devices*, vol. 61, no. 11, pp. 3871–3876, Nov. 2014, doi: 10.1109/TED.2014.2353213.
[36] L. Liu, Y. Lu, and J. Guo, "On monolayer MoS_2 field-effect transistors at the scaling limit," *IEEE Trans. Electron Devices*, vol. 60, no. 12, pp. 4133–4139, Dec. 2013, doi: 10.1109/TED.2014.2377632.

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