A Simple Charge Model for Symmetric Double-Gate MOSFETs Adapted to Gate-Oxide-Thickness Asymmetry

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***Abstract*—Surface-potential-based compact charge models for symmetric double-gate metal–oxide–semiconductor field-effect transistors (SDG-MOSFETs) are based on the fundamental assumption of having equal oxide thicknesses for both gates. However, for practical devices, there will always be some amount of asymmetry between the gate oxide thicknesses due to process variations and uncertainties, which can affect device performance significantly. In this paper, we propose a simple surface-potential-based charge model, which is applicable for tied double-gate MOSFETs having same gate work function but could have any difference in gate oxide thickness. The proposed model utilizes the unique so-far-unexplored quasi-linear relationship between the surface potentials along the channel. In this model, the terminal charges could be computed by basic arithmetic operations from the surface potentials and applied biases, and thus, it could be implemented in any circuit simulator very easily and extendable to short-channel devices. We also propose a simple physics-based perturbation technique by which the surface potentials of an asymmetric device could be obtained just by solving the input voltage equation of SDG devices for small asymmetry cases. The proposed model, which shows excellent agreement with numerical and TCAD simulations, is implemented in a professional circuit simulator through the Verilog-A interface and demonstrated for a 101-stage ring oscillator simulation. It is also shown that the proposed model preserves the source/drain symmetry, which is essential for RF circuit design.**

***Index Terms*—Circuit simulation, compact modeling, double-gate (DG) MOSFET, terminal charge.**

I. Introduction

Double-gate (DG) metal–oxide–semiconductor field-effect transistors (MOSFETs) have appeared as a replacement for bulk MOSFETs in sub-32-nm technology nodes [1]–[4]. Existing surface-potential-based compact models [5] for symmetric DG MOSFETs (SDG-MOSFETs) are based on the fundamental assumption that both gates have equal oxide thickness. For practical devices, it is most likely that the thicknesses of the two gate oxides are slightly different due to process variations and uncertainties, which can affect device performance significantly. Analysis of asymmetric DG (ADG)-MOSFETs is difficult as the input voltage equations (IVEs) of ADG are far more complicated than those of SDG [6], and their implementation in a circuit simulator is not trivial [7].

In this paper, we propose a simple surface-potential-based charge model applicable for tied DG-MOSFETs having same gate work function but could have any difference in the thickness of the gate oxides. The proposed model utilizes the unique quasi-linear relationship of surface potentials of the two gates along the channel that has been so far unexplored. In this model, the analytic expressions for the terminal charges are expressed in terms of the basic arithmetic operations of the surface potentials and the applied biases (similar to surface-potential-based bulk MOSFET models), making it extremely easy to implement in any circuit simulator and small geometry effects could be added to it by a perturbation approach as done for bulk MOSFETs [8]. We also propose, for the cases of small asymmetry in gate oxide, a simple physics-based perturbation technique by which the surface potential of an ADG device could be obtained just by solving the IVE of an SDG device and, thus, eliminates the necessity to solve the IVE of ADG-MOSFETs altogether. The proposed model is shown to have excellent agreement with numerical and TCAD simulations. It is implemented in a professional circuit simulator through the Verilog-A interface and is shown to preserve the source/drain symmetry, which is essential for RF circuit design [9]. A 101-stage ring oscillator has been also successfully simulated using the proposed model.

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II. Description of the Model

A. Derivation of the Terminal Charges

Conventions used in this paper are as follows. $C_{\mathrm{ox}1(2)}$ is the oxide capacitance per unit area of the first (second) gate defined as $\epsilon_{\mathrm{ox}}/t_{\mathrm{ox}1(2)}$, and C_{si} is the silicon body capacitance per unit area defined as $\epsilon_{\mathrm{si}}/t_{\mathrm{si}}$, where ϵ_{si} and ϵ_{ox} are the permittivities and t_{si} and t_{ox} are the thicknesses of silicon and $\mathrm{SiO_2}$, respectively. q is the elementary charge; β is the inverse thermal voltage; n_i is the intrinsic carrier density; $B = 2qn_i/\beta\epsilon_{\mathrm{si}}$; $\psi_{1(2)}$ Si/$\mathrm{SiO_2}$ is the surface potential at the first (second) gate;

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V is the electron quasi-Fermi potential (channel potential); and V_g is the effective gate voltage, i.e., $V_g = V_{g_{\text{applied}}} - \delta\phi$, where $V_{g_{\text{applied}}}$ is the voltage applied at the gate terminal and $\delta\phi$ is the work-function difference of the gate material. W is the channel width, L is the channel length, and μ is the effective mobility. In all the discussion that follows, any variable with subscript "s" refers to its values at the source end and with subscript "d" refers to its value at the drain end.

The "exact" drain current through a DG-MOSFET could be written as [10]

$$I_{ds} = \mu \frac{W}{L} \left[F(Q_{i1s}, Q_{i1d}, G_s) - F(Q_{i1d}, Q_{i2d}, G_d) \right] \quad (1)$$

where

$$F(Q_{i1}, Q_{i2}, G) = \frac{Q_{i1}^2}{2C_{\text{ox1}}} + \frac{Q_{i2}^2}{2C_{\text{ox2}}} + \frac{2}{\beta}(Q_{i1}+Q_{i2}) + \frac{1}{2}\epsilon_{\text{si}} t_{\text{si}} G. \quad (2)$$

Here, Q_{i1} and Q_{i2} are the inversion charge densities of the first and second gates, respectively, given by

$$Q_{i1(2)} = C_{\text{ox1(2)}} \left(V_g - \psi_{1(2)} \right) \quad (3)$$

and G, the coupling factor (always negative for the present case), is expressed as [6]

$$G = \frac{Q_{i1}^2}{\epsilon_{\text{si}}^2} - Be^{\beta(\psi_1 - V)} = \frac{Q_{i2}^2}{\epsilon_{\text{si}}^2} - Be^{\beta(\psi_2 - V)}. \quad (4)$$

It should be noted that some approximate drain current models are also available in the literature [11].

As shown in Fig. 1, the proposed charge model is based on the following two observations.

1) For any given bias condition, along the channel, the surface potentials (i.e., ψ_1 and ψ_2) hold a quasi-linear relationship. This is due to the fact that both gates are connected together and they have same work-function difference. It is imperative that Q_{i1} and Q_{i2} will also hold the same quasi-linear relationship.
2) For any given bias condition, coupling factor G is a linear function of surface potential along the channel if the MOSFET is in weak inversion or in linear operation mode. However, their relationship is highly nonlinear when the transistor is in saturation. Here, nonlinearity factor NLF is calculated as in [12]

$$NLF = \frac{\sqrt{\int_{\psi_{1s}}^{\psi_{1d}} \left[G(\psi) - \tilde{G}(\psi) \right]^2 d\psi}}{\psi_{1d} - \psi_{1s}} \quad (5)$$

where $\tilde{G}(\psi)$ is the linear approximation of the exact $G(\psi)$ given by (4). At the same time, as demonstrated on the left y-axis in Fig. 1(b), the contribution of the $\epsilon_{\text{si}} t_{\text{si}}(G_s - G_d)/2$ component in the drain current equation is significant only when the transistor is in weak inversion. Therefore, if G is always assumed to be a linear function of $\psi_{1(2)}$ or $Q_{i1(2)}$, it should not show significant error in terminal charge calculation.

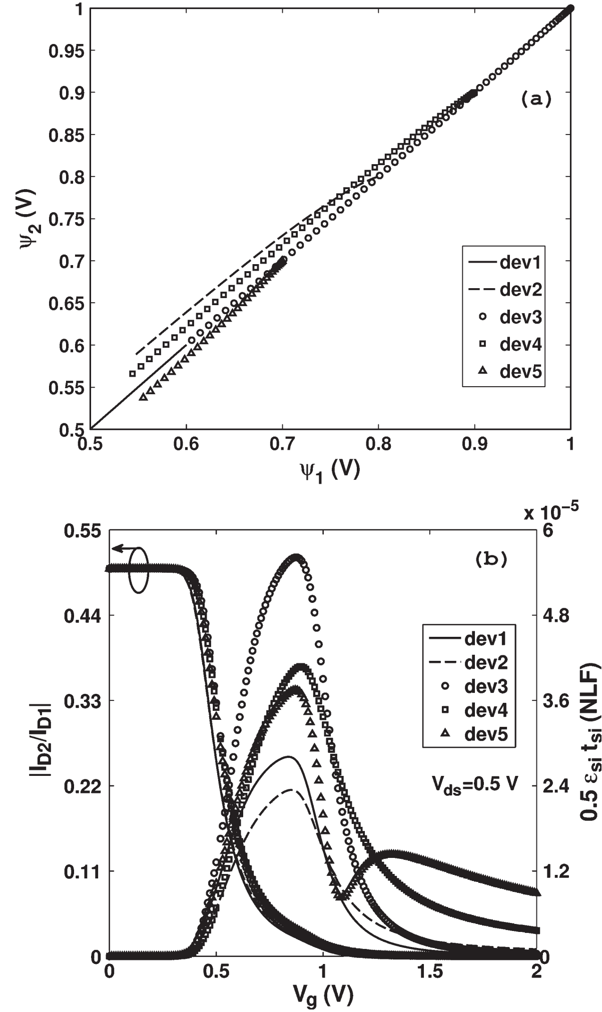

Fig. 1. (a) Quasi-linear relation between ψ_1 and ψ_2 across the channel for a variety of devices with different V_g for $V_{ds} = 2$ V. The devices used and their respective biases are as follows: dev1: $V_g = 0.6$ V, $t_{\text{ox1}} = 2$ nm, $t_{\text{ox2}} = 2$ nm, and $t_{\text{si}} = 20$ nm; dev2: $V_g = 0.9$ V, $t_{\text{ox1}} = 3$ nm, $t_{\text{ox2}} = 2$ nm, and $t_{\text{si}} = 20$ nm; dev3: $V_g = 1$ V, $t_{\text{ox1}} = 1$ nm, $t_{\text{ox2}} = 1$ nm, and $t_{\text{si}} = 10$ nm; dev4: $V_g = 0.8$ V, $t_{\text{ox1}} = 2$ nm, $t_{\text{ox2}} = 1$ nm, and $t_{\text{si}} = 10$ nm; and dev5: $V_g = 0.7$ V, $t_{\text{ox1}} = 1$ nm, $t_{\text{ox2}} = 4$ nm, and $t_{\text{si}} = 10$ nm. For the same devices, (b) on the left y-axis, shows the magnitude of term I_{D2}/I_{D1}, where $I_{D2} = \mu(W/L)\epsilon_{\text{si}} t_{\text{si}}(G_s - G_d)/2$ and $I_{D1} = I_{ds} - I_{D2}$, and on the right y-axis, it shows the nonlinearity factor NLF as a function of V_g for $V_{ds} = 0.5$ V. NLF remains low, and $|I_{D2}/I_{D1}|$ remains high in weak inversion for any V_{ds}.

Based on the above two approximations, we linearize $Q_{i2(1)}$ and G as a function of $Q_{i1(2)}$ as follows:

$$\tilde{Q}_{i2(1)} = m_{1(2)} Q_{i1(2)} + c_{1(2)} \quad (6)$$

$$\tilde{G}_{1(2)} = s_{1(2)} Q_{i1(2)} + k_{1(2)} \quad (7)$$

where

$$m_{1(2)} = \frac{Q_{i2(1)s} - Q_{i2(1)d}}{Q_{i1(2)s} - Q_{i1(2)d}} \quad (8)$$

$$c_{1(2)} = \frac{Q_{i1(2)s} Q_{i2(1)d} - Q_{i2(1)s} Q_{i1(2)d}}{Q_{i1(2)s} - Q_{i1(2)d}} \quad (9)$$

$$s_{1(2)} = \frac{G_d - G_s}{Q_{i1(2)d} - Q_{i1(2)s}} \quad (10)$$

$$k_{1(2)} = \frac{G_s Q_{i1(2)d} - G_d Q_{i1(2)s}}{Q_{i1(2)d} - Q_{i1(2)s}}. \quad (11)$$

Now, $F(Q_{i1}, Q_{i2}, G)$ could be approximated as

$$F(Q_{i1}, Q_{i2}, G) \approx F(Q_{i1}, \tilde{Q}_{i2}, \tilde{G}_1) \approx F(\tilde{Q}_{i1}, Q_{i2}, \tilde{G}_2). \quad (12)$$

Therefore, linearization helps us to approximate F as a quadratic function of Q_{i1} and Q_{i2}, as shown in (2) and (6)–(7).

If Q_{i1} and Q_{i2} be the inversion charge densities at a position y along the channel ($y = 0$ describes the source end and $y = L$ denotes the drain end), one can write [13]

$$\frac{y}{L} = \frac{F_s - F}{F_s - F_d} \quad (13)$$

where $F_s = F(Q_{i1s}, Q_{i2s}, G_s)$ and $F_d = F(Q_{i1d}, Q_{i2d}, G_d)$. Using (12) in (13), we can express y as a quadratic function of Q_{i1} and Q_{i2} as follows:

$$\frac{y}{L} = \alpha_{1(2)}\, Q_{i1(2)}^2 + \gamma_{1(2)} Q_{i1(2)} + \delta_{1(2)} \quad (14)$$

where

$$\alpha_{1(2)} = -\frac{\left[\frac{1}{2c_{\text{ox}1(2)}} + \frac{m_{1(2)}^2}{2c_{\text{ox}2(1)}}\right]}{F_s - F_d} \quad (15)$$

$$\gamma_{1(2)} = -\frac{\left[\frac{\epsilon_{\text{si}} t_{\text{si}} s_{1(2)}}{2} + \frac{2(m_{1(2)}+1)}{\beta} + \frac{c_{1(2)} m_{1(2)}}{c_{\text{ox}2(1)}}\right]}{F_s - F_d} \quad (16)$$

$$\delta_{1(2)} = \frac{F_s - \left(\frac{\epsilon_{\text{si}} t_{\text{si}} k_{1(2)}}{2} + \frac{2c_{1(2)}}{\beta} + \frac{c_{1(2)}^2}{2c_{\text{ox}2(1)}}\right)}{F_s - F_d}. \quad (17)$$

Using Ward–Dutton charge partition theory [14], the terminal charges could be computed as

$$\begin{aligned} Q_G &= W \sum_{k=1}^{2} \left[\int_{Q_{iks}}^{Q_{ikd}} Q_{ik} \frac{dy}{dQ_{ik}} dQ_{ik} \right] \\ &= WL \left[\frac{2\alpha_1}{3} \left(Q_{i1d}^3 - Q_{i1s}^3\right) + \frac{\gamma_1}{2} \left(Q_{i1d}^2 - Q_{i1s}^2\right) \right. \\ &\quad \left. + \frac{2\alpha_2}{3} \left(Q_{i2d}^3 - Q_{i2s}^3\right) + \frac{\gamma_2}{2} \left(Q_{i2d}^2 - Q_{i2s}^2\right) \right] \quad (18) \end{aligned}$$

$$\begin{aligned} Q_D &= -\frac{W}{L} \sum_{k=1}^{2} \left[\int_{Q_{iks}}^{Q_{ikd}} Q_{ik}\, y \frac{dy}{dQ_{ik}} dQ_{ik} \right] \\ &= -WL \left[\frac{2\alpha_1^2}{5} \left(Q_{i1d}^5 - Q_{i1s}^5\right) + \frac{3\gamma_1\alpha_1}{4} \left(Q_{i1d}^4 - Q_{i1s}^4\right) \right. \\ &\quad + \left(\frac{2\alpha_1\delta_1 + \gamma_1^2}{3}\right) \left(Q_{i1d}^3 - Q_{i1s}^3\right) \\ &\quad + \left(\frac{\gamma_1\delta_1}{2}\right) \left(Q_{i1d}^2 - Q_{i1s}^2\right) \\ &\quad + \frac{2\alpha_2^2}{5} \left(Q_{i2d}^5 - Q_{i2s}^5\right) + \frac{3\gamma_2\alpha_2}{4} \left(Q_{i2d}^4 - Q_{i2s}^4\right) \\ &\quad + \left(\frac{2\alpha_2\delta_2 + \gamma_2^2}{3}\right) \left(Q_{i2d}^3 - Q_{i2s}^3\right) \\ &\quad \left. + \left(\frac{\gamma_2\delta_2}{2}\right) \left(Q_{i2d}^2 - Q_{i2s}^2\right) \right] \quad (19) \end{aligned}$$

$$Q_S = -Q_G - Q_D. \quad (20)$$

It is note worthy that in (18)–(20), the terminal charges can be obtained by arithmetic operations on surface potentials and terminal voltages and could be extended to small geometry devices by a bulk transistor modeling approach [8]. The proposed model is different from the few existing charge models for the ADG-MOSFETs [15], [16] in the following aspects.

1) It utilizes the unique quasi-linear relationship of the surface potentials of the tied DG-MOSFETs having same gate work function. This property has remained unexplored so far and might be useful in the future to model and characterize such device properties. It should be noted that the earlier work [16] was based on an empirical relationship between Q_i and y.
2) In another work [15], [17], effective charge $\hat{Q}_k = (\sum_k Q_{ik}) \times (dV/d\psi_k)$ is being linearized with respect to the surface potential instead of actual inversion charge Q_{ik}. However, it is difficult to control the numeric precision of $\hat{Q}_k$ since, in the weak inversion region (which is a common case at the drain end), $(\sum_k Q_{ik}) \to 0$ and $dV/d\psi_k \to \infty$, which leads to additional effort in their robust implementation. It should be noted that $G \to 0$ at weak inversion and IVE has discontinuity at $G = 0$.

B. Analytical Approximation of Surface Potential

In order to calculate an approximate value of the surface potential in the case of gate-oxide-thickness asymmetry, we first calculate the exact surface potential ψ_0 of a symmetric device explicitly [18] having gate oxide thickness of $t_{\text{ox}1}$ (in case of asymmetry, we always assign a smaller gate oxide thickness to $t_{\text{ox}1}$ to improve accuracy). Now, we use the trigonometric IVEs of the asymmetric device [6] to calculate the first-order surface potential perturbation due to the oxide thickness asymmetry. The analytical expressions for $\partial\psi_1/\partial C_{\text{ox}2}$ and $\partial\psi_2/\partial C_{\text{ox}2}$ obtained from [6, eqs. (12) and (14)], respectively, are shown below

$$\left.\frac{\partial\psi_1}{\partial C_{\text{ox}2}}\right|_{\psi_1=\psi_0} = \frac{Q_{i0}}{C_{\text{ox}1}(\lambda_1\xi_1 + \lambda_2\xi_2)} \quad (21)$$

$$\left.\frac{\partial\psi_2}{\partial C_{\text{ox}2}}\right|_{\psi_1=\psi_0} = \frac{\lambda_1\sigma_1 + \lambda_2\sigma_2}{\lambda_1\xi_1 + \lambda_2\xi_2} \quad (22)$$

where

$$\lambda_1 = \frac{C_{\text{ox}1} Q_{i0}}{\epsilon_{\text{si}}^2} + \frac{\beta}{2}\Upsilon \quad (23)$$

$$\lambda_2 = C_{\text{ox}1} + \frac{\beta\, Q_{i0}}{2} \quad (24)$$

$$\sigma_1 = \frac{-Q_{i0}^2 \chi}{\epsilon_{\text{si}} C_{\text{ox}1} G} \quad (25)$$

$$\sigma_2 = \frac{2\sigma_1}{\beta\epsilon_{\text{si}}\chi} \quad (26)$$

$$\xi_1 = -\left(\frac{\epsilon_{\text{si}}\lambda_1\,\chi}{G} + \frac{\epsilon_{\text{si}}^2}{Q_{i0}}\right) \quad (27)$$

$$\xi_2 = -\frac{2\lambda_1}{\beta G} \quad (28)$$

and $Q_{i0} = C_{\text{ox1}}(V_g - \psi_0)$, $\Upsilon = B\, e^{\beta(\psi_0 - V)}$, and $\chi = t_{\text{si}} + (2\epsilon_{\text{si}}/\beta\, Q_{i0}$. Using the Taylor series expansion to first order, the surface potentials for the asymmetric device can be approximated as

$$\psi_1 \approx \psi_0 + \left.\frac{\partial \psi_1}{\partial C_{\text{ox2}}}\right|_{\psi_1=\psi_0} (C_{\text{ox2}} - C_{\text{ox1}}) \tag{29}$$

$$\psi_2 \approx \psi_0 + \left.\frac{\partial \psi_2}{\partial C_{\text{ox2}}}\right|_{\psi_2=\psi_0} (C_{\text{ox2}} - C_{\text{ox1}}). \tag{30}$$

Although one can obtain ψ_2 explicitly from ψ_1, we have not used such relationship as it is valid under certain solution space, and thus, an approximate value of ψ_1 does not *mathematically guarantee* a real value for ψ_2.

The proposed perturbation technique is shown to yield good results with reasonable accuracy for an asymmetry up to 50% in oxide thickness. This is much simpler than the perturbation technique [19] reported earlier, which uses an additional solution of IVE for symmetric devices and more computationally intensive correction terms.

III. Results and Discussion

We validate the proposed models with the results of exact numerical integration of (18) and (19) and also with TCAD simulations [20]. The modern compact models are implemented in circuit simulator in charge based approach in order to satisfy the charge conservation. However the charge models are conventionally verified in terms of transcapacitance values, as any error in terminal charge calculation is magnified due to the presence of the derivative term in transcapacitance expressions [15]. As mentioned in [21], there are four independent capacitance values for a tied-gate DG-MOSFET, namely, C_{gg}, C_{dg}, C_{gd}, and C_{dd}. Fig. 2 shows the plot of these four transcapacitance values for two different devices, i.e., one an SDG device with $t_{\text{ox1}} = 1$ nm, $t_{\text{ox2}} = 1$ nm, and $t_{\text{si}} = 10$ nm and the other with $t_{\text{ox1}} = 1$ nm, $t_{\text{ox2}} = 3$ nm, and $t_{\text{si}} = 20$ nm. A very good match is seen for high and low V_{ds} and V_g for both the devices. In this figure, the transcapacitance values were calculated using the surface potential obtained by solving the trigonometric IVE for asymmetric devices [7].

Fig. 3(a) and (b) shows the plot of drain current and transcapacitance values C_{gg} and C_{dg} for different extents of t_{ox2} variation over t_{ox1} for a nominal SDG device. Surface potentials needed to compute drain current, and transcapacitance values are obtained using the perturbation technique proposed in this brief. One can see that the perturbation technique yields excellent agreement with the exact results obtained using real oxide thicknesses for small asymmetry cases and the TCAD data. One can also note that there is a significant change in drain current and transcapacitance values due to gate-oxide-thickness asymmetry, which necessitates the inclusion of asymmetry effects in symmetric DG models.

Fig. 3(c) shows the error in computation of ψ_1 and ψ_2 using the proposed perturbation technique. It can be seen that the

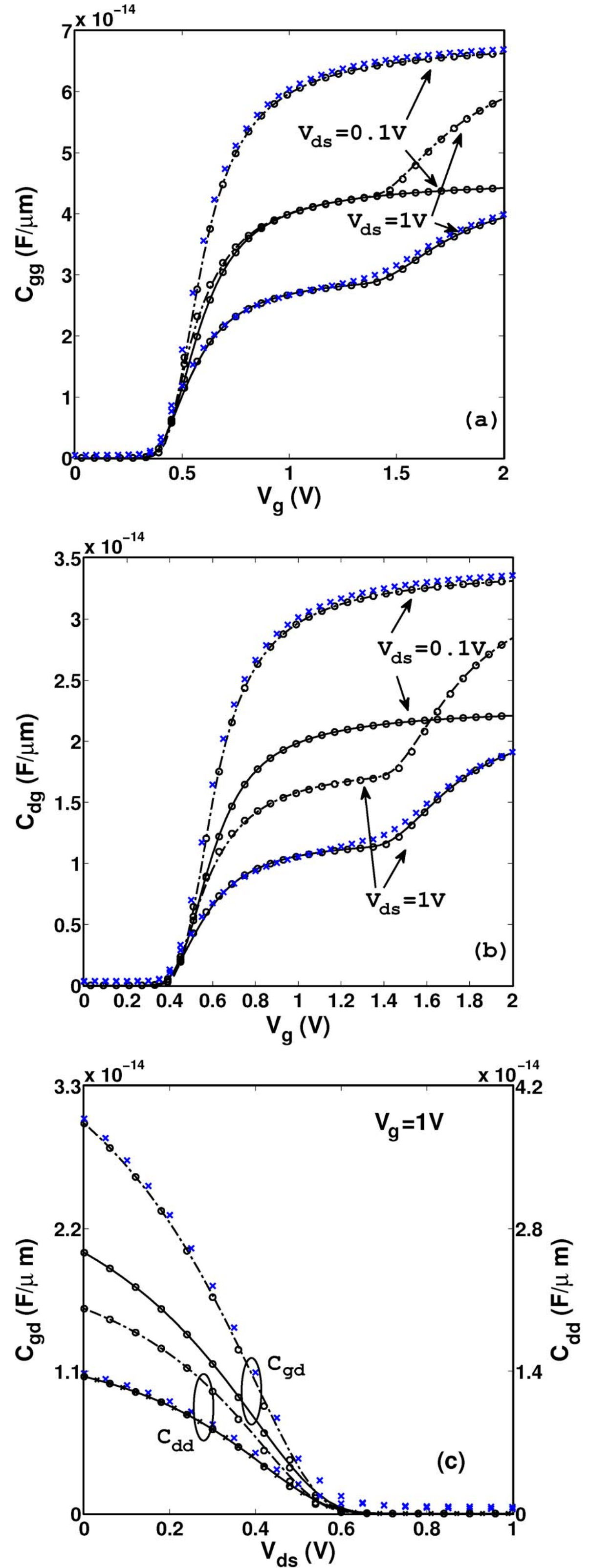

Fig. 2. Different transcapacitance characteristics predicted by the proposed model for two devices with device parameters (dotted line) $t_{\text{ox1}} = 1$ nm, $t_{\text{ox2}} = 1$ nm, and $t_{\text{si}} = 10$ nm and (solid line) $t_{\text{ox1}} = 1$ nm, $t_{\text{ox2}} = 3$ nm, and $t_{\text{si}} = 20$ nm, as well as the corresponding exact values obtained from (circles) numerical simulation and (crosses) TCAD simulation. To keep the clarity of the figure, TCAD data have been put for few cases.

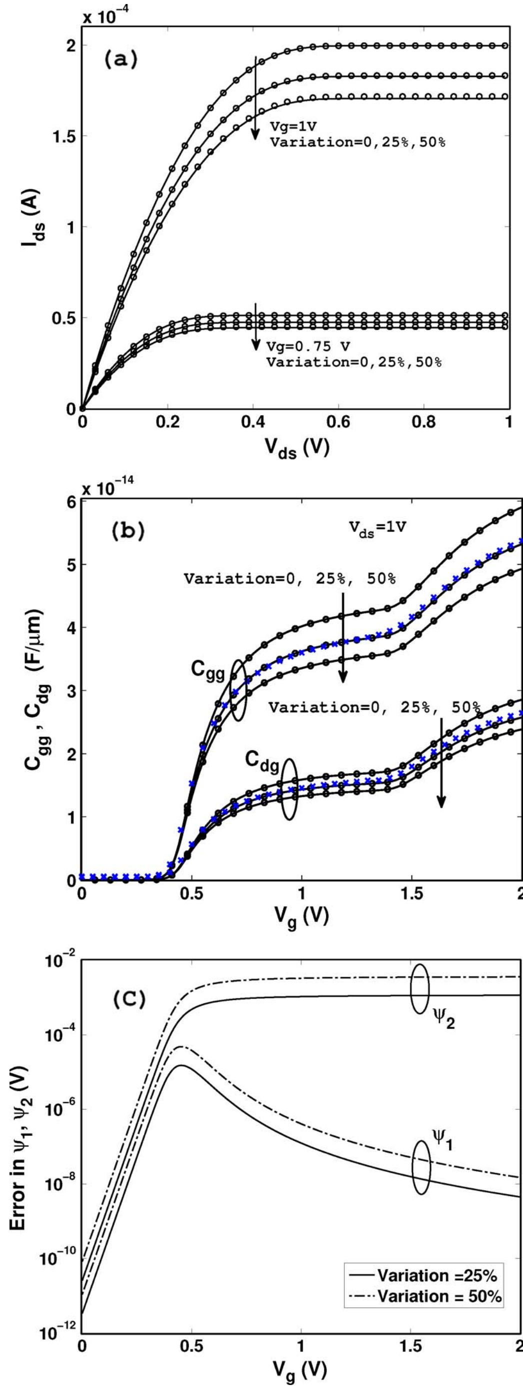

Fig. 3. (a) and (b) Comparison of drain current I_{ds} and transcapacitance values C_{gg} and C_{dg} predicted using the perturbation technique (lines) with the exact value obtained using real oxide values (circles) and TCAD (crosses) for different extents of t_{ox2} variation over t_{ox1}. (c) Error in ψ_1 and ψ_2 prediction using the proposed perturbation technique. The nominal device used has parameters $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 1$ nm and $t_{\mathrm{si}} = 10$ nm.

dominant surface potential ψ_1 is obtained with much more accuracy than ψ_2 since it is closer to ψ_0, the surface potential of the symmetric device, over which perturbation is applied. As we assign the smaller capacitance to t_{ox1}, the proposed perturbation technique is quite accurate since the device properties are mainly controlled by ψ_1 rather than ψ_2.

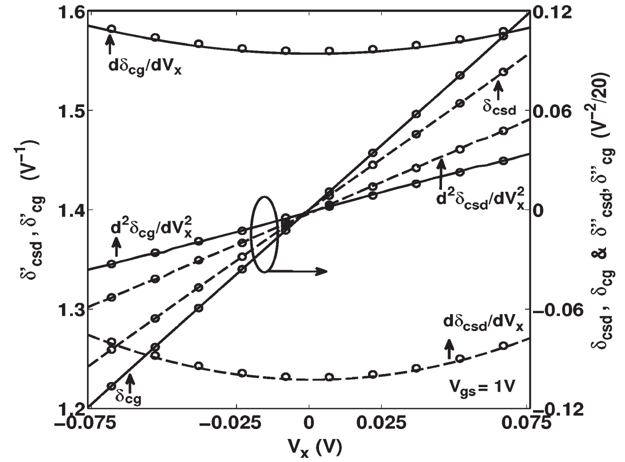

Fig. 4. Source–drain symmetry test for the proposed charge model as obtained from the circuit simulator, i.e., SmartSpice version 4.3.2.c, for a device with parameters $t_{\mathrm{ox1}} = 1$ nm, $t_{\mathrm{ox2}} = 1.3$ nm, and $t_{\mathrm{si}} = 10$ nm. Continuity of (solid line) δ_{cg} and (dotted line) δ_{csd} and their first and second derivatives with respect to V_x at $V_x = 0$ assure source–drain symmetry. Here, the second derivatives, i.e., δ''_{cg} and δ''_{csd}, are scaled down by a constant factor of 20 to fit the axis. (δ_{cg}, δ_{csd}, and V_x are defined in [9].) The lines denote simulation using the perturbation technique applied on a nominal SDG device with parameters $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 1$ nm and $t_{\mathrm{si}} = 10$ nm, and the symbols denote simulation using the exact value of surface potentials obtained using real oxide values.

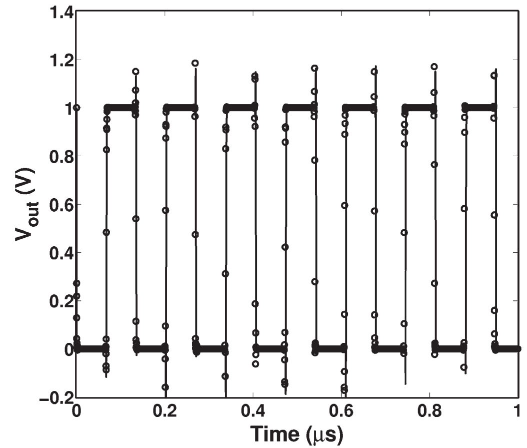

Fig. 5. Simulated transient characteristics of a 101-stage ring oscillator using a circuit simulator, i.e., SmartSpice version 4.3.2.c. The W/L ratio of a pMOSFET is kept three times of the nMOSFET with device parameters $t_{\mathrm{ox1}} =$ 1 nm, $t_{\mathrm{ox2}} = 1.3$ nm, and $t_{\mathrm{si}} = 10$ nm being same for both. The lines denote simulation using the proposed perturbation technique applied on a nominal SDG device with parameters $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 1$ nm and $t_{\mathrm{si}} = 10$ nm, whereas the symbols denote simulation using the exact value of surface potentials obtained using real oxide values. A constant electron mobility value of 300 $\mathrm{cm}^2/\mathrm{V\cdot sec}$ and hole mobility of 100 $\mathrm{cm}^2/\mathrm{V\cdot sec}$ is used in calculating currents.

We implemented our model in a professional circuit simulator [22] through its Verilog-A interface and conducted a source/drain symmetry test as suggested in [9]. Fig. 4 shows that the proposed charge model has successfully passed the symmetry test, which is essential for RF circuit design. We adopted the technique similar to [23] to maintain the model continuity in the neighborhood of $V_{ds} = 0$. A 101-stage ring oscillator has been successfully simulated, the waveform of which is shown in Fig. 5.

IV. Conclusion

We have proposed a simple surface-potential-based charge model that is applicable for tied DG-MOSFETs having same gate work function but could have any difference in gate oxide thickness. In the proposed model, which exploits the unique quasi-linear relationship between the surface potentials along the channel, the terminal charges could be computed by basic arithmetic operations from the surface potentials and applied biases, and thus, it is much simpler than the existing models. We have also proposed a simple physics-based perturbation technique by which the surface potentials of an asymmetric device could be obtained just by solving the IVE of SDG devices for small asymmetry cases. The proposed model, which shows excellent agreement with numerical and TCAD simulations, is implemented in a professional circuit simulator through the Verilog-A interface and is shown to preserve the source/drain symmetry, which is essential for RF circuit design.

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