Assessment of SET Logic Robustness Through Noise Margin Modeling

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***Abstract*—A compact model for noise margin (NM) of single-electron transistor (SET) logic is developed, which is a function of device capacitances and background charge (ζ). Noise margin is, then, used as a metric to evaluate the robustness of SET logic against background charge, temperature, and variation of SET gate and tunnel junction capacitances (C_G and C_T). It is shown that choosing $\alpha = C_T/C_G = 1/3$ maximizes the NM. An estimate of the maximum tolerable ζ is shown to be equal to $\pm 0.03e$. Finally, the effect of mismatch in device parameters on the NM is studied through exhaustive simulations, which indicates that $\alpha \in [0.3, 0.4]$ provides maximum robustness. It is also observed that mismatch can have a significant impact on static power dissipation.**

***Index Terms*—Background charge, compact model, Coulomb blockade, noise margin (NM), single-electron transistor (SET).**

I. Introduction

SINGLE-ELECTRON transistor (SET) has attracted a lot of attention as an emerging nanotechnology due to its ultralow power dissipation, new functionalities, nanofeature size, and CMOS compatible fabrication process [1]–[3]. Significant amount of research has been carried out on implementing digital circuits and memories using single-electron devices [6]–[9]. It is, therefore, very essential to study the noise margin (NM) in SET logic.

There are two main approaches to design logic gates using single electronics. One approach is based on using SET as a MOS-like switch and trying to mimic CMOS gates; this approach is known as voltage-state approach [2], [11], [12]. Another paradigm of computation is to encode a state by the presence or absence of an electron, which is known as single-electron encoded logic or charge-state approach [6]. Though the latter has more potential, as it is faster and leads to lower power dissipation, it requires load capacitances to be in the order of SET device capacitances (attofarad or less), which is probably not feasible in real applications. The former approach, although slower, is not limited by such constraint, and hence, is attractive for practical applications. Our analysis in this paper is only for voltage-state approach, which we refer to as SET logic.

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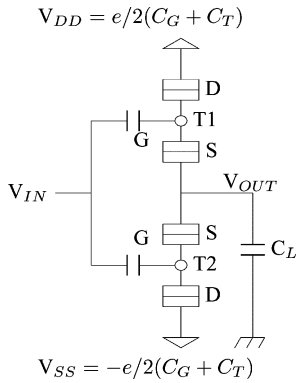


Fig. 1. SET-based inverter, C_L is the output load capacitance.

The main contributions of this paper are: 1) proposal of a new model for the NM of SET inverter in terms of device capacitances and background charge and 2) analysis of the robustness of SET inverter using NM as a metric. The Mahapatra–Ionescu–Banerjee (MIB) model [10] along with couple of smart assumptions are used to derive analytical expression for NM, which is compact and accurate. We show mathematically that $\alpha\,(C_T/C_G)$ is the most important parameter while designing SET circuits for robustness, and $\alpha = 1/3$ maximizes NMs. We also obtain a limit for maximum allowable background charge that the SET logic can tolerate, and it is found to be $\pm 0.03e$. We show that maximum mismatch in device capacitance is limited to $\pm 10\%$. Korotkov *et al*. [14] have earlier reported similar bounds for temperature and background charge, which SET logic can tolerate; however, those results were mostly empirical in nature.

II. SET Inverter

The schematic of a SET inverter is shown in Fig. 1. Here, C_G and C_T are the gate capacitance and source/drain junction tunnel capacitance [10] (we assume that source and drain tunnel junctions are symmetrical, $C_{\rm TD} = C_{\rm TS} = C_T$). The inverter was first proposed by Tucker [11], and later, modified by Likharev *et al*. [12], [13]. The SET-based inverter resembles CMOS inverter; however, there are two main differences [1]:

1) Both the push ($T1$) and pull ($T2$) transistors are identical to each other, unlike CMOS-based inverter.
2) Dual supply voltage is required, and the supply ($V_{\rm DD}$ and $V_{\rm SS}$ in Fig. 1) is defined by the gate and tunnel capacitances.

The static characteristics of the SET inverter are shown in Fig. 2. It is apparent from the characteristics that the voltage levels in the logic high and logic low are not constant. The static

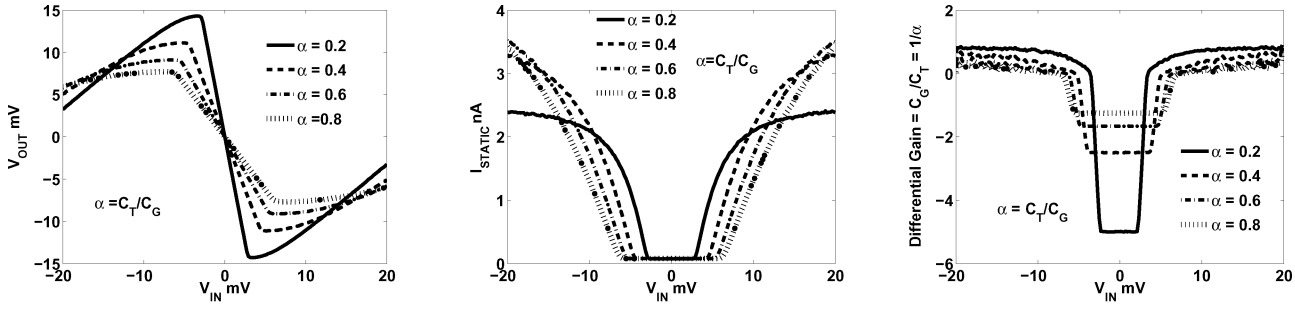


Fig. 2. SET inverter characteristics. (Simulated with $V_{\rm DD} = -V_{\rm SS} = 20$ mV $\Rightarrow C_G + C_T = 4$ aF, source and drain junction tunnel resistances $R_{\rm TS} = R_{\rm TD} = 1$ MΩ and $T = 3$ K.) (a) Voltage transfer characteristics. (b) Current characteristics. (c) Differential gain characteristics.

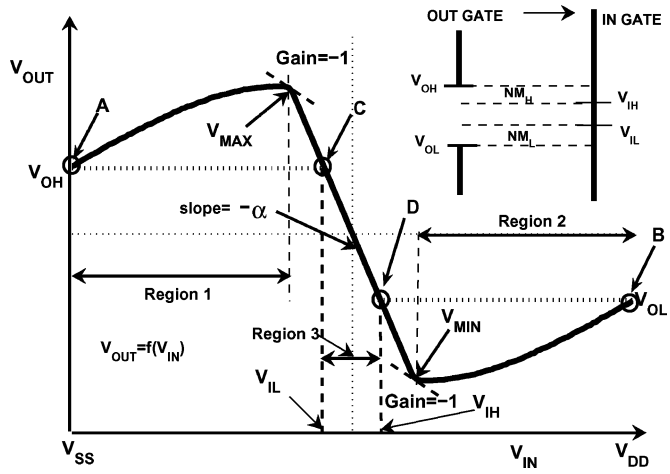


Fig. 3. SET logic NM.

current characteristics indicate that the current from $V_{\rm DD}$ to $V_{\rm SS}$ in the logic transition region is minimum, which is complementary to what is observed in a CMOS inverter, where there is a current surge in this region. The differential gain in the logic transition region is given by $-1/\alpha = -C_G/C_T$, which is much smaller when compared to the CMOS inverter.

III. Derivation of Noise Margin

In the following derivation of the NM, we assume that the devices $T1$ and $T2$ (see Fig. 1) are identical, which is reasonable and also helps to keep the the algebra simple.

The choice of $V_{\rm OH}$ and $V_{\rm OL}$ (points A and B in Fig. 3) for the SET inverter is obvious, because anything above $V_{\rm OH}$ should be a logic 1 and A is the only point that satisfies this; similar argument is also valid for point B. The input–output relation for the "Region 1" (see Fig. 3) is given by the following equation, which is derived from the MIB compact model for SET [10]. The following equations are valid for $T \ll e^2/C_\Sigma K_B$ and zero background charge, where $C_\Sigma = C_G + 2C_T$

$$V_{\rm out}^3 + A_2 V_{\rm out}^2 + A_1 V_{\rm out} + A_0 = 0 \tag{1}$$

where

$$A_2 = \frac{C_G(e/2 + C_G V_{\rm IN})}{C_T(C_G + C_T)} \tag{2}$$

$$A_1 = \frac{-\left(e^2/4 + \left(C_G C_T + C_T^2 + C_G^2\right)V_{\rm DD}^2 + eC_G V_{\rm IN} + C_G^2 V_{\rm IN}^2\right)}{C_T(C_G + C_T)} \tag{3}$$

$$A_0 = \frac{C_G V_{\rm DD}^2 (e/2 + C_G V_{\rm IN})}{C_T(C_G + C_T)}. \tag{4}$$

The order of C_G and C_T is in attofarad, and the voltage levels are in the order of millivolts, hence, we can neglect the cubic and the square terms in (1).[1]

Making the earlier assumptions, (1) becomes linear

$$A_1 V_{\rm out} + A_0 = 0. \tag{5}$$

Now, to obtain $V_{\rm OH}$, we substitute $V_{\rm IN} = V_{\rm SS} = -e/2(C_G + C_T)$ in (3)–(4) to obtain new values of A_1 and A_0, using these in (5), we obtain

$$V_{\rm OH} = \frac{1}{2}\frac{eC_G C_T}{(C_G + C_T)\left(C_G^2 + C_G C_T + 2C_T^2\right)}. \tag{6}$$

Similarly, substituting $V_{\rm IN} = V_{\rm DD} = e/2(C_G + C_T)$ in (3)–(4), we obtain the expression for $V_{\rm OL}$ as

$$\begin{aligned} V_{\rm OL} &= -\frac{1}{2}\frac{eC_G C_T}{(C_G + C_T)\left(C_G^2 + C_G CT + 2C_T^2\right)} \\ &= -V_{\rm OH}. \end{aligned} \tag{7}$$

The choice of $V_{\rm IH}$ and $V_{\rm IL}$ is critical. In the case of CMOS inverter, $V_{\rm IN}$ at gain $= -1$ is taken as $V_{\rm IL}$ and $V_{\rm IH}$. The fundamental definition of $V_{\rm IL}$ is the maximum input voltage that can be fed to the inverter so that the output is a logic high ($\geq V_{\rm OH}$). Hence, $V_{\rm IL}$ can be found by solving $V_{\rm IL} = f^{-1}(V_{\rm OH})$ [where $V_{\rm out} = f(V_{\rm in})$ in Fig. 3]. The slope of the logic transition region "Region 3" is $-C_G/C_T$ [1], hence

$$\begin{aligned} V_{\rm IL} &= -\frac{C_T}{C_G}V_{\rm OH} \\ &= -\frac{1}{2}\frac{eC_T^2}{(C_G + C_T)\left(C_G^2 + C_G C_T + 2C_T^2\right)}. \end{aligned} \tag{8}$$

[1]It turns out that A_2 is of the order of 10^{-3}, and hence, $A_2 V_{\rm out}^2$ can be neglected for the device parameters under consideration.

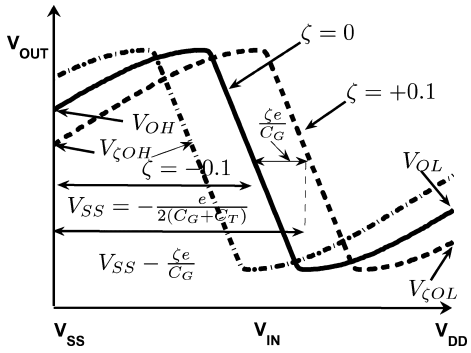


Fig. 4. Effect of background charge (ζ) on inverter characteristics, the background charge causes inverter characteristics to shift laterally by an amount $\zeta e/C_G$, positive value of ζ shifts the characteristics to the right, $V_{\rm OH}\downarrow, V_{\rm IH}\uparrow \Rightarrow {\rm NM}_H \Downarrow; V_{\rm OL}\downarrow, V_{\rm IL}\uparrow \Rightarrow {\rm NM}_L \Uparrow$.

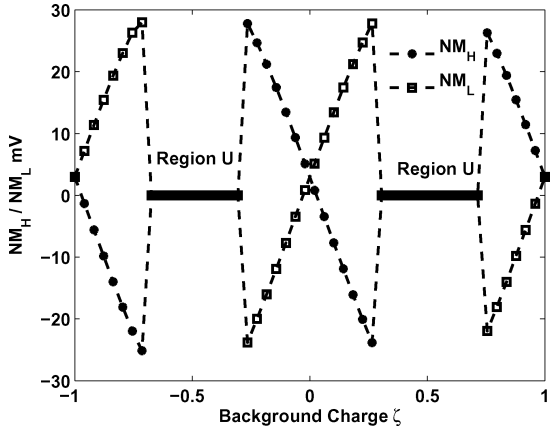


Fig. 5. Effect of background charge (ζ) on NM (${\rm NM}_H$/${\rm NM}_L$).

Similarly, $V_{\rm IH}$ is the minimum input voltage that needs to be fed to the inverter so that the output is a logic low ($\leq V_{\rm OL}$). Hence, $V_{\rm IH} = f^{-1}(V_{\rm OL})$

$$V_{\rm IH} = \frac{C_T}{C_G}V_{\rm OL} = \frac{1}{2}\frac{eC_T^2}{(C_G+C_T)(C_G^2+C_GC_T+2C_T^2)}. \quad (9)$$

The definition of NM is

$${\rm NM}_L = V_{\rm IL} - V_{\rm OL}, \quad {\rm NM}_H = V_{\rm OH} - V_{\rm IH}. \quad (10)$$

From (6) to (10), and using $\alpha = C_T/C_G$

$${\rm NM}_H = {\rm NM}_L = (1-\alpha)\frac{V_{\rm DD}}{1/\alpha + 2\alpha + 1}. \quad (11)$$

The above expressions give results, which are within 10% of what were obtained from simulation using SIMON [21] [a widely used Monte Carlo (MC) simulator for single-electron devices]. Model of NM (11) is developed for very low temperatures and its validity for higher temperature will be discussed in Section VI.

IV. Modeling of Background Charge Effect

The effect of background charge on the SET inverter is to shift the inverter characteristics laterally, as shown in Fig. 4. The lateral shift causes changes in $V_{\rm OH}$ and $V_{\rm OL}$, which, in turn, affects $V_{\rm IL}$ and $V_{\rm IH}$, thus, affects the NMs, ${\rm NM}_H$ and ${\rm NM}_L$ [from (8), (9) and (10)].

The effect of background charge on NM, which is qualitatively shown in Fig. 5, are twofold: first, the change in NM is linear with respect to background charge. Second, it is symmetric around $\zeta =$ integer, therefore it suffices to do the analysis around $\zeta = 0$. There are regions in Fig. 5 labeled as "Region U," where the SET inverter cannot be used, as it, no longer, performs inverting action, and thus, definition of NM does not hold here. The changes in ${\rm NM}_H$ and ${\rm NM}_L$ are complimentary for variation in background charge. There is only a small window of allowable background charge that the SET inverter can tolerate such that both ${\rm NM}_H$ and ${\rm NM}_L$ are positive.

From Fig. 4, it is observed that background charge translates the transfer characteristics along the $V_{\rm IN}$ axis. To find $V_{\rm IH}$ in the presence of background charge, we need to evaluate A_1 and A_0 at $V_{\rm IN} = V_{\rm SS} - (\zeta e/C_G)$. This is because, the origin ($V_{\rm IN}$ corresponding to $V_{\rm out} = 0$) translates to $\zeta e/C_G$ in the presence of background charge; hence, $A_{\zeta 1}$ and $A_{\zeta 0}$ can be calculated using expressions for A_1 and A_0 [(3)–(4)] with $V_{\rm IN} = V_{\rm SS} - (\zeta e/C_G)$, hence

$$A_{\zeta 0} = \frac{e^3C_G(C_T - 2(C_G+C_T)\zeta)}{8C_T(C_G+C_T)^4} \quad (12)$$

$$A_{\zeta 1} = -e^2\big(C_G^2 + C_GC_T + 2C_T^2 - 4C_T(C_G+C_T)\zeta + 4(C_G+C_T)^2\zeta^2\big)/4C_T(C_G+C_T)^3. \quad (13)$$

Using (12) and (13) in (5) and simplifying, we get

$$V_{\zeta\rm OH} = eC_G(C_T - 2(C_G+C_T)\zeta)/2\big((C_G+C_T)\big(C_G^2+C_GC_T + 2C_T^2 - 4C_T(C_G+C_T)\zeta + 4(C_G+C_T)^2\zeta^2\big)\big). \quad (14)$$

Dropping the ζ dependent terms in the denominator of (14)[2] and rearranging, we get the following expression for $V_{\zeta\rm OH}$

$$V_{\zeta\rm OH} = V_{\rm OH}\left\{1 - 2\left(1+\frac{1}{\alpha}\right)\zeta\right\}. \quad (15)$$

One could go through a similar argument to arrive for an expression for $V_{\zeta\rm OL}$ in "Region 2" in Fig. 5

$$V_{\zeta\rm OL} = -V_{\rm OH}\left\{1 + 2\left(1+\frac{1}{\alpha}\right)\zeta\right\}. \quad (16)$$

Since $V_{\zeta\rm IL} = f^{-1}(V_{\zeta\rm OH})$ and $V_{\zeta\rm IH} = f^{-1}(V_{\zeta\rm OL})$, we need to find the relation between $V_{\rm out}$ and $V_{\rm in}$ in "Region 3" in the presence of ζ. Region 3 can be expressed as a straight line by

$$V_{\rm IN} = \frac{C_T}{C_G}\left(\frac{\zeta e}{C_T} - V_{\rm out}\right). \quad (17)$$

[2]Since the value of ζ is <0.4, the quadratic term of ζ can be neglected. The resulting linear expression introduces some error, which is, later, corrected by using a fitting parameter in the final expression for NM.

Substituting $V_{\rm out} = V_{\zeta \rm OL}$ in (17), we get

$$V_{\zeta \rm IH} = \frac{C_T}{C_G}\left(\frac{\zeta e}{C_T} - V_{\zeta \rm OL}\right). \tag{18}$$

Using (16) in (18), we have

$$V_{\zeta \rm IH} = \frac{\zeta e}{C_G} + \frac{C_T}{C_G} V_{\rm OH}\left(1 + 2\left(1 + \frac{1}{\alpha}\right)\zeta\right). \tag{19}$$

Since $\rm NM_{\zeta H} = V_{\zeta OH} - V_{\zeta IH}$, using (15) and (19), we have

$$\rm NM_{\zeta H} = NM_H - \left(\frac{e}{C_G} + 2V_{\rm OH}\left(2 + \alpha + \frac{1}{\alpha}\right)\right)\zeta. \tag{20}$$

Similarly, $\rm NM_{\zeta L}$ can be derived as

$$\rm NM_{\zeta L} = NM_H + \left(\frac{e}{C_G} + 2V_{\rm OH}\left(2 + \alpha + \frac{1}{\alpha}\right)\right)\zeta. \tag{21}$$

An empirical parameter[3] $\gamma = 0.9825$ is introduced to correct the slope of (20) and (21) to account for the approximations made in (15). Finally, we have

$$\begin{aligned} \rm NM_{\zeta H} &= \rm NM_H - \gamma\left(\frac{e}{C_G} + 2V_{\rm OH}\left(2 + \alpha + \frac{1}{\alpha}\right)\right)\zeta \\ \rm NM_{\zeta L} &= \rm NM_H + \gamma\left(\frac{e}{C_G} + 2V_{\rm OH}\left(2 + \alpha + \frac{1}{\alpha}\right)\right)\zeta \\ \gamma &= 0.9825. \end{aligned} \tag{22}$$

The error associated with the earlier model is less than 10% for a wide range of supply voltages and α ratios.

V. Maximizing Noise Margin and Maximum Allowable Background Charge $\zeta_{\rm MAX}$

From (11), we can find an optimal α to maximize NMs by setting the derivative of $\rm NM_H$ to zero

$$3\alpha^2 + 2\alpha - 1 = 0 \Rightarrow \alpha = \frac{1}{3}. \tag{23}$$

This is verified by simulations, as shown in Fig. 6.

From (22), the maximum allowable background charge $\zeta_{\rm MAX}$ can be obtained as (equating $\rm NM_{\zeta H} = 0$)

$$\zeta_{\rm MAX} = \frac{1}{4\gamma}\frac{\alpha(1-\alpha)}{(1+\alpha)(1+\alpha+\alpha^2)}. \tag{24}$$

An optimal α can be found in order to maximize $\zeta_{\rm MAX}$ by differentiating (24) and setting it to zero

$$\alpha^4 - 2\alpha^3 - 4\alpha^2 - 2\alpha + 1 = 0. \tag{25}$$

Solving (25) numerically, we get $\alpha = 0.2988$.[4] Using this value of α in (24), we get $\zeta_{\rm MAX} = 0.0296e$ (where e is the fundamental unit of charge $= 1.6 \times 10^{-19}$ C). It is interesting to note that earlier Korotkov *et al*. [14] have made an empirical estimate for $\zeta_{\rm MAX} = 0.1e$, the reason for discrepancy may be due to the fact that in their work they have assumed the gain of the inverter as the deciding metric.

[3]The fitting parameter is obtained by dividing the actual slope, found by simulation to the slope predicted by (20) and (21), and averaging it over a wide spectrum of supply voltage and α values. We have varied supply voltage from 10 to 100 mV in steps of 10 mV, and for each value of supply voltage, we have varied α from 0.1 to 1 in steps of 0.1 to calculate the fitting parameter.

[4]The equation has four roots $-0.8229 + 0.5628i$, $-0.8229 - 0.5628i$, 0.2988, and 3.3470. We are not interested in $\alpha = 3.3470$, because the gain in the transition region of the inverter becomes less than 1.

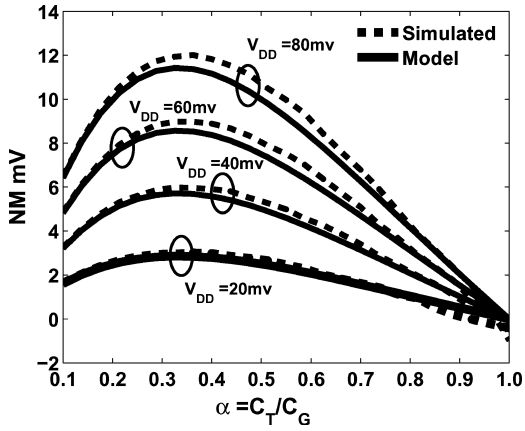


Fig. 6. NM variation with α, NM is maximum at $\alpha = 1/3$, as predicted by (11). The proposed model is verified by simulations with SIMON [21].

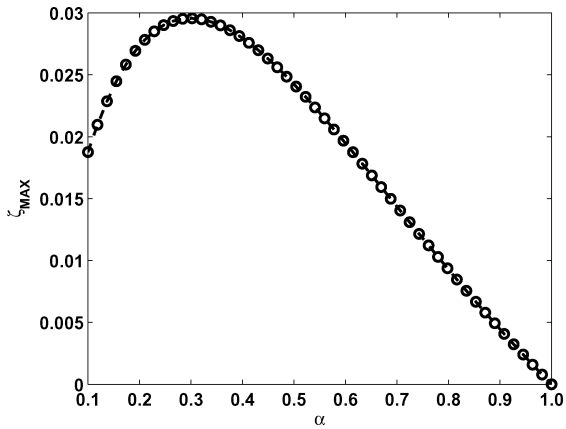


Fig. 7. $\zeta_{\rm MAX}$ versus α.

It is interesting to note from (24) that $\zeta_{\rm MAX}$ only depends on the ratio of $C_T/C_G = \alpha$ and not on absolute values of C_G or C_T, making it independent of supply voltage $V_{\rm DD}$ or $V_{\rm SS}$. The maximum allowable background charge ($|\zeta_{\rm MAX}|$) is $\approx 0.03e$ when the inverter has $\alpha \approx 0.3$. Variation of $\zeta_{\rm MAX}$ with respect to α is shown in Fig. 7. We have verified the expression for $\zeta_{\rm MAX}$ (24) by simulating a chain of inverters with a distribution of background charge (see Fig. 8). It is interesting to observe that after ten stages, the voltage levels settle to ± 10 mV, indicating robustness against ζ.

VI. Effect of Temperature on the NM

The effect of temperature on the NM is illustrated in Fig. 9. Increasing temperature tends to decrease $V_{\rm MAX}$ (increase $V_{\rm MIN}$); however, it does not affect $V_{\rm OH}$ and $V_{\rm OL}$ [see Fig. 9(a)]. Since $V_{\rm IH} = \alpha V_{\rm OL}$ ($V_{\rm IL} = \alpha V_{\rm OH}$), NMs do not change much with temperature unless it is very high (simulated at $V_{\rm DD} =$ 20 mV, $\alpha = 0.4$). Normally, one would like $E_C \gg K_B T$ to observe single-electron charging effects (where $E_C = e^2/C_\Sigma$ is the charging energy [2]). From Fig. 9, we can see that NM

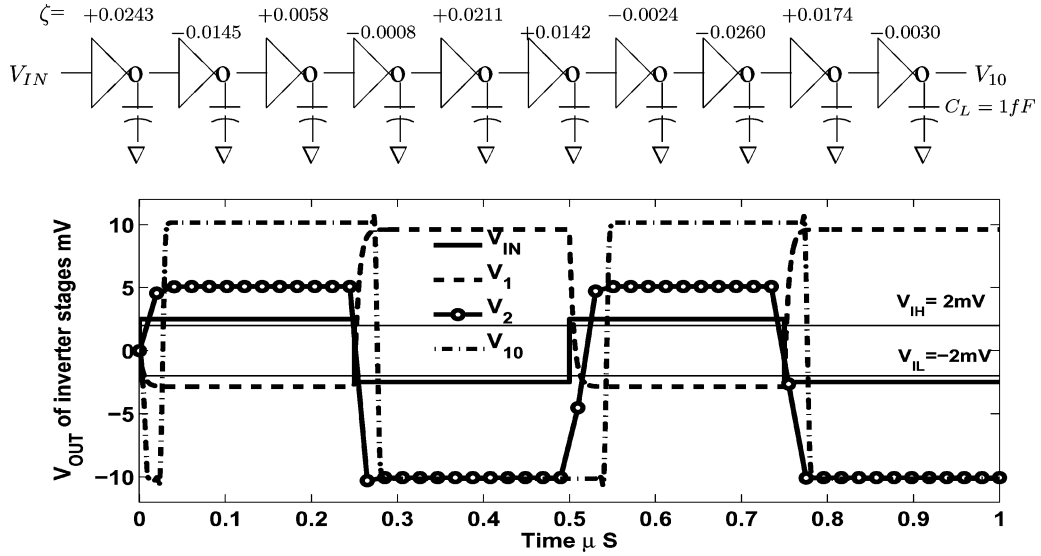
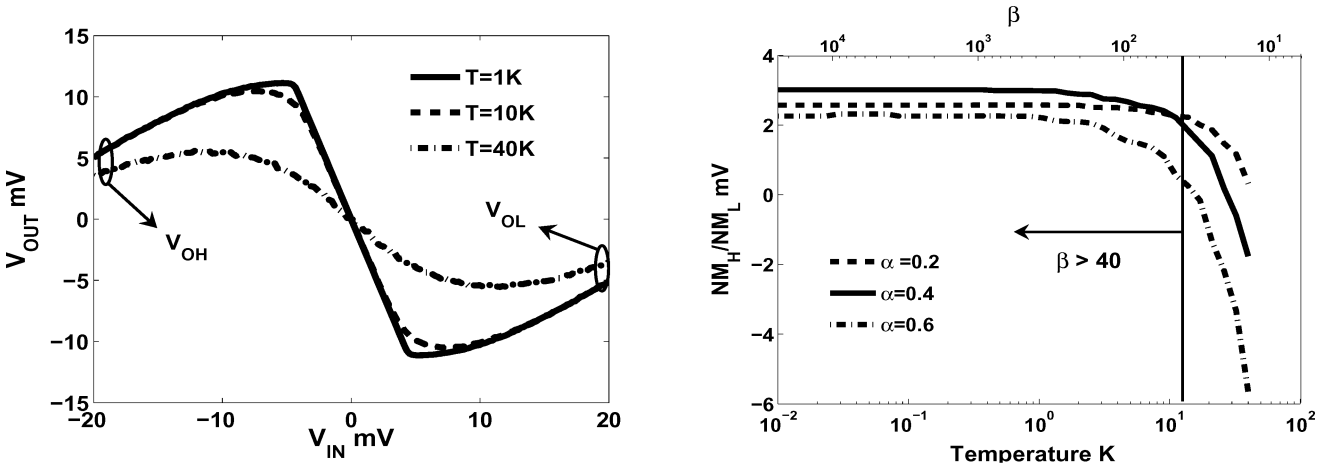


Fig. 8. Simulation of a chain of SET inverters with $V_{\rm DD} = -V_{\rm SS} = 20$ mV, $\alpha = 0.4$, $R_{\rm TS} = R_{\rm TD} = 1$ MΩ and each inverter having a nonzero ζ; the top inset shows the distribution of ζ on each inverter. This simulation was done by porting MIB model into Eldo [22] Verilog-A environment.



(a) (b)

Fig. 9. Effect of temperature on NM in all simulations $C_G + C_T = 4$ aF and $R_{\rm TS} = R_{\rm TD} = 1$ MΩ. (a) Variation of voltage transfer characteristic with temperature. (b) Effect of temperature and $C_G : C_T$ ratio on NM.

remains almost constant till $T < e^2/40k_B C_\Sigma$. It should be noted that earlier Kirihara [19] also proposed the same limitation for SET logic operation. Korotkov *et al.* [14] also have obtained the same limit using different criterion. It is again observed that the minimal deviation in the NMs with change in temperature is for $\alpha = 0.4$ (see Fig. 5) (simulated at $V_{\rm DD} = 20$ mV).

VII. Effect of Device Parameter Variation on the NM

The effect of variation of device parameters on the NM are studied through exhaustive simulations. It is observed that the variation in device capacitances C_T and C_G have a considerable impact on the NM because Coulomb blockade is controlled by device capacitances. The impact of simultaneous variation of capacitance in both the SETs $T1$ and $T2$ (see Fig. 1), with $V_{\rm DD}$ fixed is studied. Choosing $\alpha = 0.4$ gives maximum immunity to capacitance variation [see Fig. 10(b)], an increase in the NM for a negative capacitance variation is observed for $\alpha = 0.2, 0.4$, this is attributed to the increase in $V_{\rm OH}$ [see Fig. 10(a)]. If $\alpha = 0.4$, we observe that we can have a maximum variation of up to 30% before the NM degrade to 0, this is independent of the supply voltage [see Fig. 10(c)]. It is also observed that capacitance variation can have a huge impact on static power dissipation [see Fig. 10(a)], increase in capacitance leads to the increase in $P_{\rm STATIC}$ $((V_{\rm DD} - V_{\rm SS})I_{\rm STATIC})$, because the transistors are pushed out of Coulomb blockade regime (simulated at $V_{\rm DD} = 20$ mV, for $\alpha = 0.4$).

We also study the effect of mismatch between $T1$ and $T2$, mismatch in $T1$ ($T2$) leads to skewing of $\rm NM_H$ and $\rm NM_L$. Positive mismatch in $T1$ ($T2$) results in an increase $\rm NM_L$ ($\rm NM_H$), which can directly be attributed to the spread in the transfer characteristics [see Fig. 11(a)] near $V_{\rm OL}$ regions. $\alpha = 0.4$ again turns out to be the optimal point to operate Fig. 11(b). The maximum mismatch between $T1$ and $T2$ is limited to 10% [see Fig. 11(c)] (both $\rm NM_H, NM_L \geq 0$) [simulated with $V_{\rm DD} =$ 20 mV, $\alpha = 0.4$ for Fig. 11(a); $V_{\rm DD} = 20$ mV for Fig. 11(b)].

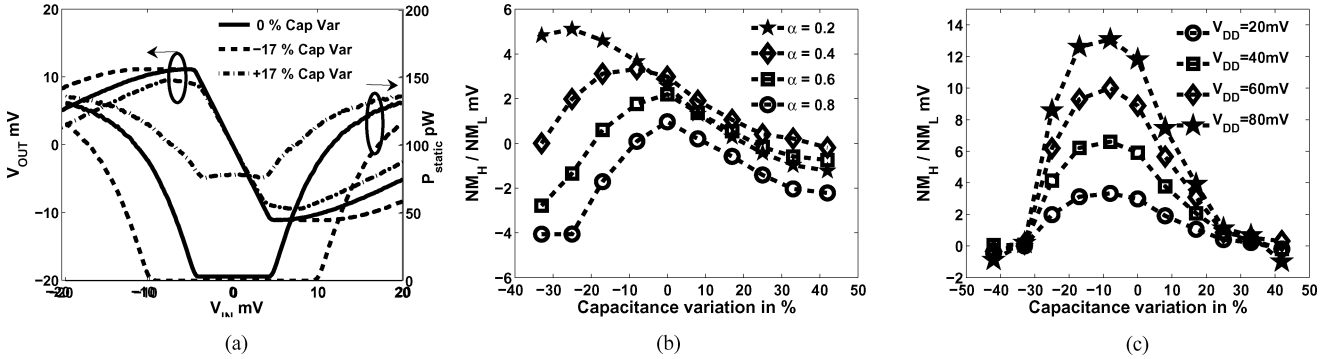


Fig. 10. Effect of capacitance variation on the NM. (a) Inverter characteristics along with power dissipation. (b) Effect of capacitance variation on the NM margin at $V_{\rm DD} = 20$ mV for different α. (c) Effect of capacitance variation on the NM with $\alpha = 0.4$.

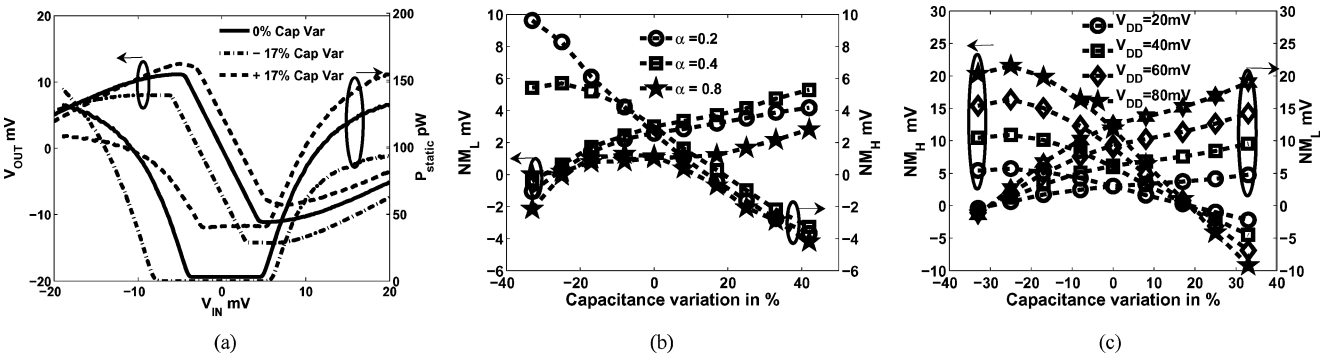


Fig. 11. Study of mismatch between $T1$ and $T2$. (a) Transfer characteristic with the variation in $T1$ only. (b) Effect of mismatch of $T1$ on the NM. (c) Effect of mismatch of $T1$ on the NM with $\alpha = 0.4$.

It is observed that variation of tunnel junction resistance ($R_{\rm TS}, R_{\rm TD}$) has almost no impact on NM, it only changes propagation delay and power dissipation [18].

VIII. Comparison With CMOS Logic

In CMOS logic we have ideal $V_{\rm OH} \approx V_{\rm DD}$ and $V_{\rm OL} \approx 0$. This gives CMOS logic high NMs and makes CMOS immune to noise. The current study shows that the maximum NM in SET is of the order of $V_{\rm DD}/6$, for $\alpha = 1/3$ (11), which is quite small if compared to CMOS inverters. The intrinsic noise levels in SET is reported to be very small [23], which can boost the robust performance of SET logic in spite of their poor NMs.

The output of an inverter can be expressed as

$$V_{\rm out} = f(V_{\rm in} + V_{\rm noise}) \tag{26}$$

using first-order Taylor series approximation

$$V_{\rm out} = f(V_{\rm in}) + \frac{dV_{\rm out}}{dV_{\rm in}} V_{\rm noise} \tag{27}$$

where $V_{\rm noise}$ represents noise voltage, the choice of $V_{\rm IL}$ and $V_{\rm IH}$ points in CMOS inverter makes sure that the gain is less than 1 in logic states high and low, this helps in filtering noise, which is apparent from (27). The SET logic may be unstable (dynamically) in the region between $V_{\rm MAX}$ and $V_{\rm IL}$ ($V_{\rm IH}$ and $V_{\rm MIN}$) (see Fig. 3), as this region corresponds to logic high (low) where the gain is greater than 1. The extent of instability may not be very alarming as the gain in SET logic is not very high.

The applicability of the model and tolerance values, that we report in this paper, to other gates in the SET logic family requires further investigation. This is because, unlike MOS transistor, SET does not behave like a classical electronic switch. The SET is basically a nonlinear device whose unique Coulomb blockade oscillation properties are cleverly exploited to make logic gates. In OFF state (under Coulomb blockade), SETs in a circuit act like capacitive divider rather than (MOS like) high resistive (open circuit) components. As a result, when we try to realize other gates (NAND, NOR, etc.) [12], [13] by mimicking their CMOS counter parts, it turns out that the characteristics of these gates are not symmetric. It is also found that SET NAND (NOR) gate passes "1" ("0") strongly and "0" ("1") weakly. Therefore, unlike CMOS logic, models developed for SET inverter cannot be directly applicable for other gates. Modeling NM for other SET gates is quite complicated, each gate may have different $V_{\rm OH}$, $V_{\rm OL}$, $V_{\rm IH}$, and $V_{\rm IL}$. Now, to compute $\rm NM_{\it H}$, in general, we need to find minimum $V_{\rm OH}$ (among all possible gates and all possible conditions), and maximum $V_{\rm IH}$. In this paper, we have only considered the SET inverter, and our analysis is based on that. Therefore, the numbers we quote for different tolerance values might be slightly optimistic for other gates.

Finally, from the above discussions, it appears that although the SET logic offers lower power dissipation and smaller size, its speed, voltage gain, and robustness are inferior to the CMOS counterpart. But in nanoscale regime, where traditional CMOS power dissipation is quite high, one might think about the hybridization of SET and MOSFET for optimum performance as

suggested by Uchida *et al*. [7]. It is worth noting that "charge-based logic" is much faster and consumes lower power than "voltage-based logic." However, practical implementation of such logic and their interfacing with CMOS blocks is very difficult and requires more detailed study.

IX. Conclusion

We define the static NM for the SET inverter and derive a compact model for the same in terms of device capacitances and background charge. We show that $\alpha = C_T/C_G$ is the most important parameter for SET logic design. Choosing $\alpha \in [0.3, 0.4]$ maximizes NMs, and increases robustness to temperature, background charge (ζ), capacitance variation, and mismatch. We also show that the maximum allowable background charge in SET logic is limited to $\pm 0.03e$, and maximum mismatch in device capacitances is limited to 10%.

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