Large-Signal Model for Independent DG MOSFET

Pankaj Kumar Thakur and Santanu Mahapatra, *Senior Member, IEEE*

***Abstract*—In this paper, we show the limitations of the traditional charge linearization techniques for modeling terminal charges of the independent double-gate metal–oxide–semiconductor field-effect transistors. Based on our recent computationally efficient Poisson solution for independent double gate transistors, we propose a new charge linearization technique to model the terminal charges and transcapacitances. We report two different types of quasistatic large-signal models for the long-channel device. In the first type, the terminal charges are expressed as closed-form functions of the source- and drain-end inversion charge densities and found to be accurate when the potential distribution at source end of the channel is hyperbolic in nature. The second type, which is found to be accurate in all regimes of operations, is based on the quadratic spline collocation technique and requires the input voltage equation to be solved two more times, apart from the source and drain ends.**

***Index Terms*—Charge linearization, compact modeling, independent double-gate metal–oxide–semiconductor field-effect transistors (IDG MOSFETs), terminal charge, transcapacitance.**

I. Introduction

THE independent double-gate metal–oxide–semiconductor field-effect transistor (IDG MOSFET) has received considerable attention in recent years due to its ability to dynamically modulate threshold voltage and transconductance. So far, few analytical models [1]–[8] are proposed for IDG MOSFETs. However, to the best of our knowledge, no quasistatic large-signal model has been proposed, which is the integral part of any realistic compact model. This case is probably because of the asymmetric nature of electrostatic potential, making it difficult to linearize the inversion charge [9], which is the fundamental step for developing efficient large-signal models.

In this paper, we show that the charge linearization techniques used so far in professional compact models [10]–[12] might not be suitable for modeling terminal charges of the generalized IDG MOSFETs. Based on the computationally efficient Poisson solution [1], we propose a new charge linearization technique for modeling the terminal charges and transcapacitances. We report two different quasistatic large-signal modeling schemes for the long-channel IDG MOSFET. In the first scheme, the terminal charges are expressed as closed-form functions of the source- and drain-end inversion charge densities and are found to be accurate when the potential distribution at the source end of the channel is hyperbolic in nature. The second scheme, which is found to be accurate in all regimes of operations, is based on the quadratic spline collocation technique and requires the input voltage equations (IVEs) to be solved two more times, aside from the source and drain ends.

Manuscript received July 2, 2010; revised September 3, 2010 and September 17, 2010; accepted September 30, 2010. Date of publication November 9, 2010; date of current version December 27, 2010. This work was supported in part by the Department of Science and Technology (DST) of India under Grant SR/S3/EECE/047/2008. The review of this paper was arranged by Editor H. S. Momose.

The authors are with the Nano Scale Device Research Laboratory, Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore 560 012, India (e-mail: pkthakur@cedt.iisc.ernet.in; santanu@cedt.iisc.ernet.in).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2010.2085083

II. Limitations of Conventional Charge Linearization Schemes

Let us conceive an undoped (or lightly doped) body long-channel IDG MOSFET where L is the channel length, W is the channel width, μ is the effective mobility, $C_{\mathrm{oxf}(b)}$ is the oxide capacitance per unit area of front(back)-gate defined as $\epsilon_{\mathrm{ox}}/t_{\mathrm{oxf}(b)}$, $\varepsilon_{\mathrm{si}}$, $\varepsilon_{\mathrm{ox}}$ are the permittivities, and t_{si} and t_{ox} are the thicknesses of silicon and SiO_2, respectively. q is the elementary charge, β the is inverse thermal voltage, n_i is the intrinsic carrier density, V is the electron quasi-Fermi potential (channel potential), $\psi_{f(b)}$ Si/SiO_2 is the interface potential at $x = \mp t_{\mathrm{si}}/2$, with $x = 0$ being the center of the Si film, and $V_{\mathrm{gsf}(b)}$ is the effective front(back)-gate voltage, i.e., $V_{\mathrm{gsf}(b)} = V_{\mathrm{gsf}(b)\mathrm{applied}} - \Delta\phi_{f(b)}$, where $\Delta\phi_{f(b)}$ is the work function difference at the respective gates.

The proposed charge linearization technique is based on our recent paper on the Poisson solution for IDG MOSFETs [1], which consists of the complementary expressions of the electrostatic potential for the biased conditions $V_{\mathrm{gsf}} \geq V_{\mathrm{gsb}}$ and $V_{\mathrm{gsf}} < V_{\mathrm{gsb}}$. Note that another independent recent publication [13] has also proposed the explicit formulation of critical voltage, which decides between the trigonometric or hyperbolic solution. The main difference between [1] and [13] is that the solution in [13] depends on coupled implicit IVEs. Due to space limitations, we explain our modeling technique only for the case of $V_{\mathrm{gsf}} \geq V_{\mathrm{gsb}}$. It is imperative that the same technique remains applicable to the other case.

The rigorous (exact) drain current (I_d) model of an IDG MOSFET as proposed by Liu *et al.* [3] can also be written as

$$I_d = I_{\mathrm{df}} + I_{\mathrm{db}} \tag{1}$$

where

$$I_{\mathrm{df}} = \mu\frac{W}{L}\left[\left\{\frac{Q_{\mathrm{ifs}}^2}{2C_{\mathrm{oxf}}} + \frac{2}{\beta}Q_{\mathrm{ifs}}\right\} - \left\{\frac{Q_{\mathrm{ifd}}^2}{2C_{\mathrm{oxf}}} + \frac{2}{\beta}Q_{\mathrm{ifd}}\right\}\right] - \frac{2\mu\epsilon_{\mathrm{si}}W}{\beta L}\int_{V_s}^{V_d}\sqrt{G}d\left[sin(h)^{-1}\alpha\right] \tag{2}$$

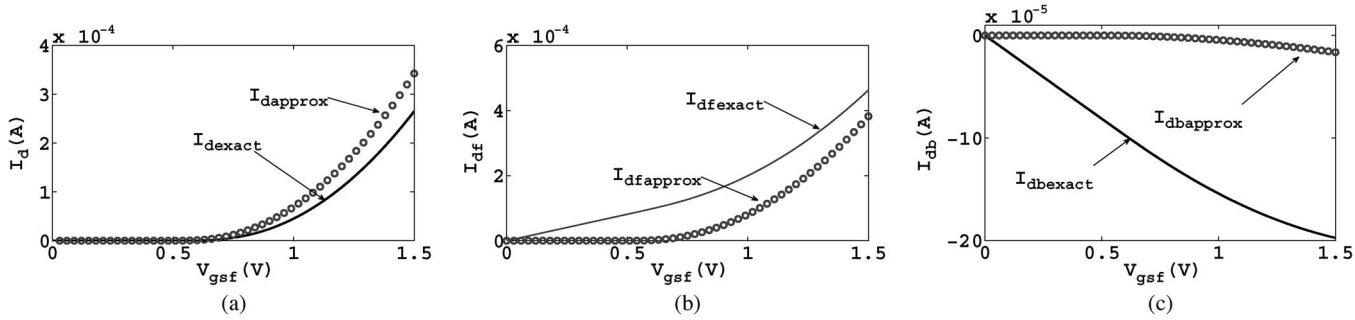

Fig. 1. Exact drain current $I_{\rm dexact}$ and the approximated drain current $I_{\rm dapprox}$ as numerically obtained. $I_{\rm dapprox}$ are calculated from (1)–(3), excluding the G and integral terms. The device parameters are $t_{\rm oxf} = 1$ nm, $t_{\rm oxb} = 2$ nm, and $t_{\rm si} = 10$ nm, and the bias voltages are $V_{\rm ds} = 1$ V, $V_{\rm gsb} = 0$ V.

$$I_{\rm db} = \mu \frac{W}{L}\left[\left\{\frac{Q_{\rm ibs}^2}{2C_{\rm oxb}} + \frac{2}{\beta}Q_{\rm ibs}\right\} - \left\{\frac{Q_{\rm ibd}^2}{2C_{\rm oxb}} + \frac{2}{\beta}Q_{\rm ibd}\right\}\right] + \mu\frac{W}{2L}\epsilon_{\rm si}t_{\rm si}(G_s - G_d) + \frac{2\mu\epsilon_{\rm si}W}{\beta L}\int_{V_s}^{V_d}\sqrt{G}d\left[sin(h)^{-1}\alpha\right]. \quad (3)$$

In the aforementioned expressions, the front- and back-gate inversion charge densities are given by

$$Q_{\rm ifs(d)} = C_{\rm oxf}\left(V_{\rm gsf} - \psi_{\rm fs(d)}\right) \quad (4)$$

$$Q_{\rm ibs(d)} = C_{\rm oxb}\left(V_{\rm gsb} - \psi_{\rm bs(d)}\right) \quad (5)$$

and $\alpha = \sqrt{|G|}/\sqrt{Be^{\beta(\psi_f - V)}}$, with the coupling factor G as

$$G = \left\{\frac{C_{\rm oxf}}{\epsilon_{\rm Si}}(V_{\rm gsf} - \psi_f)\right\}^2 - Be^{\beta(\psi_f - V)}. \quad (6)$$

Here, the subscripts "s" and "d" denote the source end (where $V = V_s$) and drain end (where $V = V_d$) of the channel, $B = 2qn_i/\beta\epsilon_{\rm si}$, and the hyperbolic and the trigonometric Poisson solutions are written together as $\sin(h)$ to avoid duplication in the derivations.

According to the Ward–Dutton charge partition theory [14], terminal charges associated with front-gate, back-gate, drain, and source terminals could be given as

$$Q_{\rm gf} = W\int_0^L Q_{\rm if}(y)dy \quad (7)$$

$$Q_{\rm gb} = W\int_0^L Q_{\rm ib}(y)dy \quad (8)$$

$$Q_d = -W\int_0^L \frac{y}{L}Q_i(y)dy \quad (9)$$

$$Q_s = -(Q_{\rm gf} + Q_{\rm gb} + Q_d) \quad (10)$$

where Q_i represents the total inversion charge $(Q_{\rm if} + Q_{\rm ib})$, and y represents the direction along the channel from the source $(y = 0)$ to the drain $(y = L)$.

The main objective of charge linearization is to find closed-form solutions for the terminal charge integrals. In bulk MOSFET, the bulk charge is linearized as a function of the surface potential. For undoped (or lightly doped) body symmetric double-gate (SDG) MOSFET, in the absence of bulk charges, the inversion charge is linearized with respect to the coupling factor G (note that C_1 in [10] and θ in [11] could be shown to be equivalent to G). This step is done so, because in the case of SDG, where G is always negative, Q_i could be expressed as a sole function of G, and as $G \to 0$, $Q_i \to 0$. In the case of IDG, the challenge is twofold: 1) G could be both positive and negative, $G = 0$ denotes the crossover point between the trigonometric and the hyperbolic modes [1], and thus, the inversion charge might not be zero at this point and 2) the inversion charges cannot be expressed as a function of a single variable.

Even if, somehow, the inversion charge can be linearized against some variable, there are other issues involved. In charge-based compact models, charge linearization is used to develop the so-called "core model" in such a manner that the drain current could be approximated as a quadratic function of $Q_{\rm is}$ and $Q_{\rm id}$ [for example, see [12] for the normalized format $i_d \approx (-q_i^2 + 2q_i)|_{q_{\rm is}}^{q_{\rm id}}$]. Such an expression is invertible for a particular $Q_i(V)$ and is thus useful for obtaining the closed-form expression of $Q_i(y)$ in terms of $Q_{\rm is}$ and $Q_{\rm id}$, which leads to an explicit expression for terminal charge integrals. However, this technique is not suitable for IDG MOSFET because of the following reasons. From the terminal charge integrals, it is clear that, apart from the total drain current model (I_d), there is a similar closed-form model for $I_{\rm df}$ and $I_{\rm db}$ for obtaining analytical expressions for $Q_{\rm if}(y)$ and $Q_{\rm ib}(y)$. Unfortunately, the integral in the expression of the $I_{\rm df}$ and $I_{\rm db}$ is not solvable (the terms cancel out when $I_{\rm df}$ and $I_{\rm db}$ are added for finding I_d). If the integral and G terms are dropped from all drain current models, the desired expression is obtained. As shown in Fig. 1, although this approximation is reasonable for the total drain current, it does not even match the trends of $I_{\rm df}$ and $I_{\rm db}$. It was observed that, if the integrals are solved and $I_{\rm df}$ and $I_{\rm db}$ are expressed as a general expression for a second-degree polynomial of $Q_{\rm ifs(d)}$ and $Q_{\rm ibs(d)}$ such as $p_{20}Q_{\rm if}^2 + p_{02}Q_{\rm ib}^2 + p_{11}Q_{\rm if}Q_{\rm ib} + p_{10}Q_{\rm if} + p_{01}Q_{\rm ib} + p_{00}$, it may be possible to get a good match with exact $I_{\rm df}$ and $I_{\rm db}$, provided that the coefficient of the polynomials becomes a function of applied biases but does not solve the purpose for obtaining a closed-form expression for $Q_{\rm if}(y)$ and $Q_{\rm ib}(y)$. Note that the surface-potential-based model [11] takes a slightly different approach (here, one seeks an explicit formulation of $\psi_{f(b)}(y)$ from a

similar quadratic equation); however, one can see in (4) and (5) that the inversion charge and the surface potential are just interchangeable parameters. Therefore, we can conclude that the conventional charge linearization techniques might not be suitable for modeling terminal charges of the IDG MOSFETs.

III. Proposed Charge Linearization Scheme

In this paper, we propose to linearize the front, back, and total inversion charge as a function of y. For brevity, we introduce a parameter $\tilde{Q}$ that represents $Q_{\rm if}$, $Q_{\rm ib}$, or Q_i. The proposed linearization process involves three steps. In the first step, $\tilde{Q}$ is linearized against channel potential V around $V = V_s$ as

$$\tilde{Q}(V) = \tilde{Q}_s + \frac{\partial \tilde{Q}_s}{\partial V_s}(V - V_s). \tag{11}$$

Note that $(\partial Q_{\rm ifs}/\partial V_s) = -C_{\rm oxf}(\partial \psi_{\rm fs}/\partial V_s)$, $(\partial Q_{\rm ibs}/\partial V_s) = -C_{\rm oxb}(\partial \psi_{\rm bs}/\partial V_s)$, and $(\partial Q_i/\partial V_s) = (\partial Q_{\rm ifs}/\partial V_s) + (\partial Q_{\rm ibs}/\partial V_s)$. The expressions for $\partial \psi_{f(b)s}/\partial V_s$ could be obtained from the IVEs reported in [1] and are given in (12) and (13), with $\lambda_3 = Be^{\beta(-V_s+\psi_{\rm fs})}$, $\lambda_1 = \sqrt{\lambda_3}\sqrt{1 \mp (\lambda_3 G_s/B)}$, and $\lambda_2 = \lambda_3^{3/2}\sqrt{1 \mp (\lambda_3 G_s/B)}$. Here, the negative and positive signs represent trigonometric and hyperbolic solutions, respectively. Due to the complicated nature of the IVEs, it is difficult to accurately obtain (12) and (13) by hand calculations. We use Mathematica [15] to obtain the following formulations:

$$\begin{aligned}\frac{\partial \psi_{\rm fs}}{\partial V_s} = \big[&\beta\epsilon_{\rm si}^2\{4C_{\rm oxb}(\lambda_3 \mp G_s)\lambda_1 \\ &-2\sqrt{|G_s|}\,(\beta\epsilon_{\rm si}\lambda_2 + C_{\rm oxb} \\ &\times(\mp 2G_s + 2\lambda_3 + \beta\lambda_2 t_{\rm si}))\,cot(h)\theta \\ &+\beta\epsilon_{\rm si}G_s(\mp 2G_s + 2\lambda_3 + \beta\lambda_2 t_{\rm si})cosec(h)^2\theta\}\big] \\ \div\big[&4C_{\rm oxb}\lambda_1\{\beta\epsilon_{\rm si}^2\lambda_3 + 2C_{\rm oxf}^2(V_{\rm gsf} - \psi_{\rm fs})\} \\ &-2\sqrt{|G_s|}\{\beta^2\epsilon_{\rm si}^2\lambda_1\lambda_3(\epsilon_{\rm si} + C_{\rm oxb}t_{\rm si}) \\ &+2\beta\big(C_{\rm oxb}\big(\epsilon_{\rm si}^2(\mp G_s + \lambda_3) + C_{\rm oxf}^2\lambda_1 t_{\rm si} \\ &\times(V_{\rm gsf} - \psi_{\rm fs})\big) \\ &+C_{\rm oxf}^2\lambda_1(V_{\rm gsf} - \psi_{\rm fs})\big) \\ &+4C_{\rm oxf}^2 C_{\rm oxb}(V_{\rm gsf} - \psi_{\rm fs})\}\,cot\theta \\ &+\beta\epsilon_{\rm si}G_s\{\beta\epsilon_{\rm si}^2\lambda_3(2 + \beta\lambda_1 t_{\rm si}) + 4C_{\rm oxf}^2(V_{\rm gsf} - \psi_{f_s}) \\ &-2\beta\,(\epsilon_{\rm si}^2 G_s - C_{\rm oxf}^2\lambda_1 t_{\rm si} \\ &\times(V_{\rm gsf} - \psi_{f_s}))\,cosec(h)^2\theta\}\big]\end{aligned} \tag{12}$$

$$\begin{aligned}\frac{\partial \psi_{\rm bs}}{\partial V_s} = \Bigg[&2\lambda_1\left\{\beta\epsilon_{\rm si}^2\left(G_s \mp \lambda_3\left(1 - \frac{\partial \psi_{\rm fs}}{\partial V_s}\right)\right.\right. \\ &\left.\left.\mp 2C_{\rm oxf}^2(-V_{\rm gsf} + \psi_{\rm fs})\frac{\partial \psi_{\rm fs}}{\partial V_s}\right)\right\} \\ &+\sqrt{|G_s|}\left\{\mp\beta^2\epsilon_{\rm si}^2\lambda_1\lambda_3 t_{\rm si}\left(\frac{\partial \psi_{\rm fs}}{\partial V_s} - 1\right)\right. \\ &\mp 4C_{\rm oxf}^2\frac{\partial \psi_{\rm fs}}{\partial V_s}(V_{\rm gsf} - \psi_{\rm fs}) \\ &+2\beta\left(\epsilon_{\rm si}^2(G_s \mp \lambda_3)\left(\frac{\partial \psi_{\rm fs}}{\partial V_s} - 1\right)\right. \\ &\mp C_{\rm oxf}^2\lambda_1 t_{\rm si}\frac{\partial \psi_{\rm fs}}{\partial V_s} \\ &\left.\left.\left.\times(V_{\rm gsf} - \psi_{\rm fs})\right)\right\}cot(h)\theta\Bigg] \\ \div\big[&2\beta\epsilon_{\rm si}^2 G_s\lambda_1\big].\end{aligned} \tag{13}$$

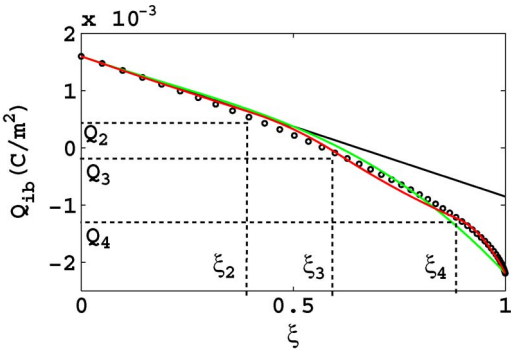

Fig. 2. Back-gate inversion charge profile along the channel for the same device parameter as in Fig. 1 with bias conditions: $V_{\rm gsf} = 1$ V, $V_{\rm gsb} = 0.6$ V, and $V_{\rm ds} = 1$ V. Here, an "o" symbol represents the numerical result, a black line represents (15), a green line represents cubic approximation, and a red line represents the spline approximation.

In the second step, the channel potential V is linearized as a function of y around $y = 0$ as follows:

$$V = V_s + \left(\frac{\partial V}{\partial y}\bigg|_{y=0}\right)y = V_s + \frac{I_d}{\mu W Q_{\rm is}}y. \tag{14}$$

Note that (11) and (14) are valid from $y = 0$ to the point of pinchoff. Using (11)–(14), the inversion charge density $\tilde{Q}$ can finally be linearized as function of y as

$$\tilde{Q}(y) = \frac{\partial \tilde{Q}_s}{\partial V_s}\frac{I_d}{\mu W Q_{\rm is}}y + \tilde{Q}_s = \tilde{n_q}y + \tilde{Q}_s. \tag{15}$$

Here, $\tilde{n_q}$ is the slope factor. It is found that (15) is valid, at least for $y \le L/2$, for any practical bias conditions.

IV. Modeling of the Terminal Charge

Using the aforementioned charge linearization technique, we propose two different models for the terminal charges.

A. Model 1

A typical inversion charge profile along the channel is shown in Fig. 2. In *model* 1, we approximate $\tilde{Q}$ as a cubic polynomial of $\xi = y/L$, e.g., $\tilde{Q} = \tilde{A}\xi^3 + \tilde{B}\xi^2 + \tilde{C}\xi + \tilde{D}$. The four polynomial coefficients $\tilde{A}$, $\tilde{B}$, $\tilde{C}$, and $\tilde{D}$ are calculated from the following four conditions:

$$\tilde{Q}(\xi = 0) = \tilde{Q}_s = \tilde{D} \tag{16}$$

$$\left.\frac{\partial\tilde{Q}(y)}{\partial\xi}\right|_{\xi=0} = \tilde{n_q} = \tilde{C} \tag{17}$$

$$\tilde{Q}(\xi=1) = \tilde{Q}_d = \tilde{A} + \tilde{B} + \tilde{C} + \tilde{D} \tag{18}$$

$$\tilde{Q}\left(\xi=\frac{1}{2}\right) = \tilde{Q}_m = \frac{\tilde{A}}{8} + \frac{\tilde{B}}{4} + \frac{\tilde{C}}{2} + \tilde{D}. \tag{19}$$

$\tilde{Q}_m$ is calculated using (15). The aforementioned four sets of equations (16)–(19) are solved to get the four coefficients, and using (7)–(10), the terminal charges are given by the following closed-form expressions:

$$Q_{\rm gf} = WL\left[\frac{A_{\rm if}}{4} + \frac{B_{\rm if}}{3} + \frac{C_{\rm if}}{2} + D_{\rm if}\right] \tag{20}$$

$$Q_{\rm gb} = WL\left[\frac{A_{\rm ib}}{4} + \frac{B_{\rm ib}}{3} + \frac{C_{\rm ib}}{2} + D_{\rm ib}\right] \tag{21}$$

$$Q_d = -WL\left[\frac{A_i}{5} + \frac{B_i}{4} + \frac{C_i}{3} + \frac{D_i}{2}\right]. \tag{22}$$

Therefore, *model* 1 is a full analytic function of $\tilde{Q}_s$ and $\tilde{Q}_d$, both of which are determined by solving the IVEs at the source and drain ends.

B. Model 2

In this technique, we seminumerically solve the terminal charge integrals. Initially, an approximation of the charge profile by the quadratic spline interpolation method is done, and then the resulting polynomial is integrated to obtain the terminal charges. The total domain $(0 \le \xi \le 1)$ is divided into four regions (i.e., three collocation points at ξ_2, ξ_3 and ξ_4, with $\xi_1 = 0$ and $\xi_5 = 1$ as shown in Fig. 2), and in each region, an approximation of the inversion charge as $\tilde{Q}(\xi) = \tilde{A}_k^2\xi^2 + \tilde{B}_k\xi + \tilde{C}_k$ is carried out, where $k = 1, 2, 3$ or 4. To keep the continuity, at each collocation point, the magnitude and the first derivative of the right and left segments have to be equal. Following this approach, the 12 polynomial coefficients are determined by solving the following 12 boundary conditions:

$$\tilde{A}_1\xi_2^2 + \tilde{B}_1\xi_2 + \tilde{C}_1 = \tilde{Q}(\xi=\xi_2) = \tilde{Q}_2 \tag{23}$$

$$\tilde{B}_1 = \left.\frac{\partial\tilde{Q}(\xi)}{\partial\xi}\right|_{\xi=\xi_1} = \tilde{n_q} \tag{24}$$

$$\tilde{C}_1 = \tilde{Q}(\xi=\xi_1) = \tilde{Q}_s \tag{25}$$

$$\tilde{A}_2\xi_3^2 + \tilde{B}_2\xi_3 + \tilde{C}_2 = \tilde{Q}(\xi=\xi_3) = \tilde{Q}_3 \tag{26}$$

$$\tilde{A}_3\xi_4^2 + \tilde{B}_3\xi_4 + \tilde{C}_3 = \tilde{Q}(\xi=\xi_4) = \tilde{Q}_4 \tag{27}$$

$$\tilde{A}_4 + \tilde{B}_4 + \tilde{C}_4 = \tilde{Q}(\xi=1) = \tilde{Q}_d \tag{28}$$

$$\tilde{A}_1\xi_2^2 + \tilde{B}_1\xi_2 + \tilde{C}_1 = \tilde{A}_2\xi_2^2 + \tilde{B}_2\xi_2 + \tilde{C}_2 \tag{29}$$

$$\tilde{A}_2\xi_3^2 + \tilde{B}_2\xi_3 + \tilde{C}_2 = \tilde{A}_3\xi_3^2 + \tilde{B}_3\xi_3 + \tilde{C}_3 \tag{30}$$

$$\tilde{A}_3\xi_4^2 + \tilde{B}_3\xi_4 + \tilde{C}_3 = \tilde{A}_4\xi_4^2 + \tilde{B}_4\xi_4 + \tilde{C}_4 \tag{31}$$

$$2\tilde{A}_1\xi_2 + \tilde{B}_1 = 2\tilde{A}_2\xi_2 + \tilde{B}_2 \tag{32}$$

$$2\tilde{A}_2\xi_3 + \tilde{B}_2 = 2\tilde{A}_3\xi_3 + \tilde{B}_3 \tag{33}$$

$$2\tilde{A}_3\xi_4 + \tilde{B}_3 = 2\tilde{A}_4\xi_4 + \tilde{B}_4. \tag{34}$$

Now, the integrals for the terminal charges (7)–(9) can be evaluated as

$$Q_{\rm gf} = \sum_{m=1}^{4} WL\left\{\frac{A_{\rm ifm}\left(\xi_{m+1}^3 - \xi_m^3\right)}{3} + \frac{B_{\rm ifm}\left(\xi_{m+1}^2 - \xi_m^2\right)}{2} + C_{\rm ifm}(\xi_{m+1} - \xi_m)\right\} \tag{35}$$

$$Q_{\rm gb} = \sum_{m=1}^{4} WL\left\{\frac{A_{\rm ibm}\left(\xi_{m+1}^3 - \xi_m^3\right)}{3} + \frac{B_{\rm ibm}\left(\xi_{m+1}^2 - \xi_m^2\right)}{2} + C_{\rm ibm}(\xi_{m+1} - \xi_m)\right\} \tag{36}$$

$$Q_d = -\sum_{m=1}^{4} WL\left\{\frac{A_{\rm im}\left(\xi_{m+1}^4 - \xi_m^4\right)}{4} + \frac{B_{\rm im}\left(\xi_{m+1}^3 - \xi_m^3\right)}{3} + \frac{C_{\rm im}\left(\xi_{m+1}^2 - \xi_m^2\right)}{2}\right\}. \tag{37}$$

The efficiency of this method depends on the optimization of choices for the collocation points. The space variable y is related to the channel potential V with the following noninvertable formulation:

$$y(V) = \frac{\mu W}{I_d}\int_{V_s}^{V} Q_i(V)dV = \frac{I_d|_{V_d=V}}{I_d|_{V_d=V_d}}. \tag{38}$$

Note that (near) exact values of $\tilde{Q}_2$, $\tilde{Q}_3$, and $\tilde{Q}_4$ are needed, and the calculation of $\tilde{Q}$ at a particular y in a straightforward method is not feasible. We chose $\xi_2 = 1/2.5$ so that $\tilde{Q}_2$ could be calculated using (15). Other two collocation points are calculated using $V = (V_0 + 0.8 \times V_P)/3$ and $V = 0.8 \times V_P$ by solving the IVEs and using (38). Here, $V_0 = (I_d/Q_{\rm is})/2.5 + V_s$ corresponds to ξ_2, and V_P is the pinchoff voltage and is calculated by equating (11) with $Q_{\rm id}$ as $V_P = (Q_{\rm is} - Q_{\rm id})/(\partial Q_{\rm is}/\partial V_s) + V_s$. These points are obtained by heuristic for the best match. However, although we need three collocation points to solve the terminal charge integrals, the proposed charge linearization technique enables solving of the IVEs only for two (ξ_3 and ξ_4). In other words, in *model* 2, we need to solve the IVEs two more times, aside from the source and drain ends of the channel. It is imperative that model accuracy increases with the number of collocation points, at the cost of computational efficiency.

V. Small Signal Model

Although it is not mandatory, from the designer's point of view, it is desirable to have an analytical formulation of small-signal parameters in a compact model. The formulation for the transconductance and conductance of IDG MOSFET is available in [2] and [16]. The closed-form expression for transcapacitances in terms of terminal charges and conductances for tied DG MOSFETs are derived in [2]. Changing the domain of the terminal charge integrals from y to V and applying

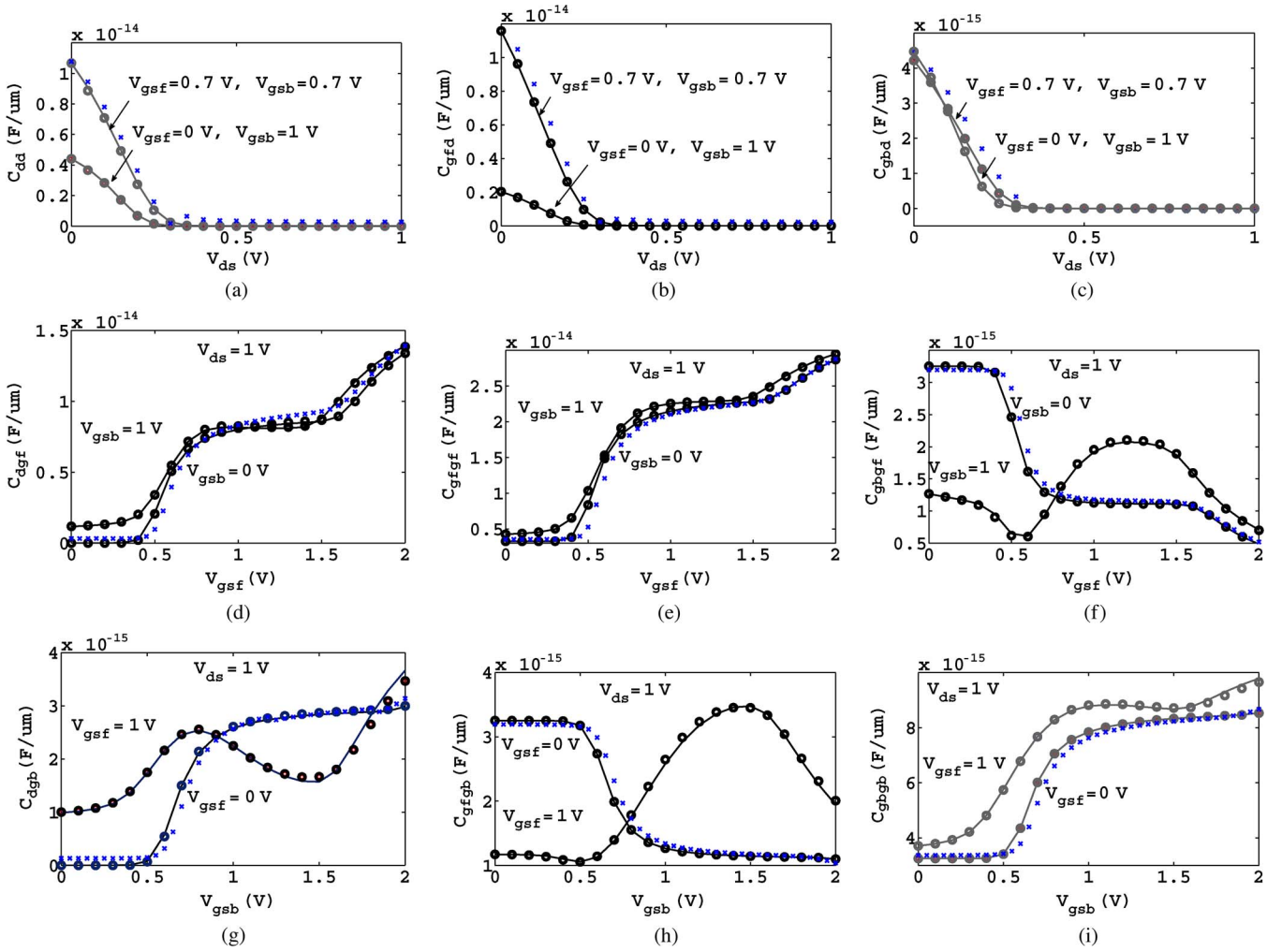

Fig. 3. Different transcapacitance characteristics obtained from *model* 2 (line) and the exact value (circle) for the device parameters $t_{\rm oxf} = 1$ nm, $t_{\rm oxb} = 3$ nm, and $t_{\rm si} = 20$ nm. In this figure, we have also shown the results obtained from the TCAD simulation [17] for a few characteristics, which are represented by the cross symbols.

the Leibnitz theorem, similar expressions for transcapacitances with respect to the source, and drain terminals could be obtained for IDG MOSFETs. However, it is difficult to get transcapacitance expressions with respect to gate terminals using the same technique, because we have two independent gates. Here, we have calculated the transcapacitance by numerically differentiating the terminal charges with respect to the terminal voltages according to the definition given in [2].

VI. Results and Discussions

We validate our model against the exact result obtained by solving the terminal charge integrals in the trapezoidal rule and also with the data obtained from the technology computer-aided design (TCAD) simulation [17]. A constant electron mobility of 300 cm^2/V-s is used. Although we have explained our modeling technique for $V_{\rm gsf} \geq V_{\rm gsb}$, here, we demonstrate our complete model, which is valid for all operating regimes. Fig. 3 shows the behavior of nine independent transcapacitances (source reference case) for different bias conditions using *model* 2, and an excellent agreement with the exact result is observed. One can also observe that the proposed model is continuous between $V_{\rm gsf} \geq V_{\rm gsb}$ and $V_{\rm gsf} < V_{\rm gsb}$ bias conditions. In Fig. 4, we compare *model* 1 with *model* 2 and observe that both models match when the Poisson solution at the source end is hyperbolic in nature; however, *model* 1 becomes inaccurate in many cases when the Poisson solution at the source end is trigonometric in nature. The reasoning behind this observation is given as follows. When the source end is in hyperbolic mode (then the drain end is also in hyperbolic mode), the signs (polarity) for $Q_{\rm if}$, $Q_{\rm ib}$, and Q_i do not change from $y = 0$ to L. However, when the source end is in trigonometric mode, the drain end could be either in trigonometric (for low V_d) or hyperbolic (for moderately high V_d), mode as explained in [1, Fig. 1(b)]. If there exists any potential minima within the body at $y = 0$ and simultaneously the drain end is in hyperbolic mode, for the $V_{\rm gsf} > V_{\rm gsb}$ case, the signs for $Q_{\rm if}$ and Q_i do not change for any value of y, but the sign for $Q_{\rm ib}$ becomes opposite at $y = 0$ and L (the scenario is reversed for the $V_{\rm gsf} < V_{\rm gsb}$ case). When the sign of $Q_{\rm ib}(y)$ changes along the channel, we found that one needs a near-exact formulation of $\tilde{Q}(y)$ to accurately predict the transcapacitance (particularly

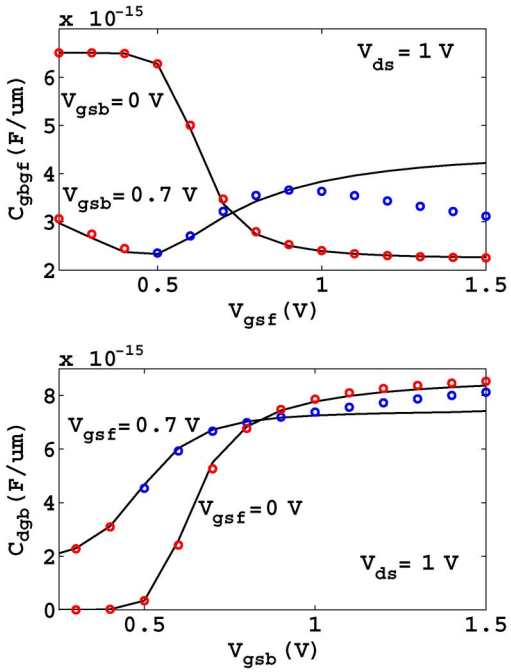

Fig. 4. Comparison of *models* 1 (line) and 2 (symbol) for the same device parameters as in Fig. 1. The "red" and "blue" colors represent that the Poisson solution at $y = 0$ is hyperbolic and trigonometric, respectively.

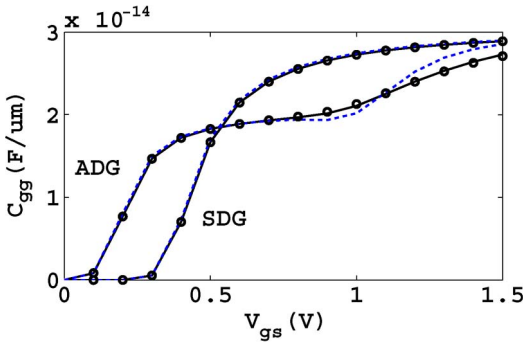

Fig. 5. Validation of *models* 1 (dotted line) and 2 (solid line) for tied double-gate transistors against the exact result (symbol). The device parameters are: $t_{\rm oxf} = 1.5$ nm, $t_{\rm oxb} = 1.5$ nm, $t_{\rm si} = 10$ nm, and $\Delta\phi_f = \Delta\phi_b = 0$ for SDG and $\Delta\phi_f = -0.56$ V and $\Delta\phi_b = 0.56$ V for ADG at $V_{\rm ds} = 2$ V.

when the $C_{\rm gfgb}$ or $C_{\rm gbgf}$ characteristics take N shape). As shown in Fig. 4, although the difference between both the models (they are different mainly at the drain side) are very small, *model* 1 cannot accurately predict the transcapacitance when the source end is in trigonometric mode. For the same reason, we believe that it is extremely difficult to develop a fully analytic terminal charge model for IDG MOSFETs, which would be accurate for all regimes of operations. In Fig. 5, we compare the performance of both models for tided double gate (symmetric and asymmetric) devices, and as we see, both models accurately predict the behavior of the SDG device, but they differ when asymmetry arises. Nevertheless, *model* 1 is useful if the designer wishes to strictly operate the device in the source end in hyperbolic mode regime for any specific reason (e.g., ultralow-power applications).

VII. Conclusion

We have proposed a new charge linearization technique for IDG MOSFETs to model the terminal charges and transcapacitances. We report two different types of modeling techniques. In the first type, the terminal charges are expressed as closed-form functions of the source- and drain-end inversion charge densities and found it to be accurate only when the potential distribution at the source end of the channel is hyperbolic in nature. The second type, which is found to be accurate in all regimes of operations, is based on the quadratic spline collocation technique and requires the IVEs to be solved two more times, apart from the source and the drain ends. All models are validated against numerical device simulators.

References

[1] A. Sahoo, P. K. Thakur, and S. Mahapatra, "A computationally efficient generalized Poisson solution for independent double-gate transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 632–636, Mar. 2010.

[2] H. Lu and Y. Taur, "An analytic potential model for symmetric and asymmetric DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1161–1168, May 2006.

[3] F. Liu, J. He, Y. Fu, J. Hu, W. Bian, Y. Song, X. Zhang, and M. Chan, "Generic carrier-based core model for undoped four-terminal double-gate MOSFETs valid for symmetric, asymmetric, and independent-gate-operation modes," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 816–826, Mar. 2008.

[4] A. S. Roy, J. M. Sallese, and C. C. Enz, "A closed-form charge-based expression for drain current in symmetric and asymmetric double gate MOSFET," *Solid State Electron.*, vol. 50, no. 4, pp. 687–693, Apr. 2006.

[5] Z. Zhu, X. Zhou, K. Chandrasekaran, S. C. Rustagi, and G. H. See, "Explicit compact surface–potential and drain–current models for generic asymmetric double gate metal–oxide–semiconductor field-effect transistors," *Jpn. J. Appl. Phys.*, vol. 46, no. 4B, pp. 2067–2072, Apr. 2007.

[6] A. Ortiz-Conde, F. J. Garcia Sanchez, J. Muci, S. Malobabic, and J. J. Liou, "A review of core compact models for undoped double-gate SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 1, pp. 131–140, Jan. 2007.

[7] G. Pei, W. Ni, A. V. Kammula, B. A. Minch, and E. C.-C. Kan, "A physical compact model of DG MOSFET for mixed-signal circuit applications—Part I: Model description," *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2135–2143, Oct. 2003.

[8] M. Reyboz, P. Martin, T. Poiroux, and O. Rozeau, "Continuous model for independent double-gate MOSFET," *Solid State Electron.*, vol. 53, no. 5, pp. 504–513, May 2009.

[9] Y. Tsividis, *Operation and Modeling of the MOS Transistor*. Boston, MA: McGraw-Hill, 1999.

[10] J.-M. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy, and C. Enz, "A design-oriented charge-based current model for symmetric and DG MOSFET and its correlation with the EKV formalism," *Solid State Electron.*, vol. 49, no. 3, pp. 485–489, Mar. 2005.

[11] G. Dessai, A. Dey, G. Gildenblat, and G. D. J. Smit, "Symmetric linearization method for double-gate and surrounding-gate MOSFETs models," *Solid State Electron.*, vol. 53, no. 5, pp. 548–556, May 2009.

[12] B. Diagne, F. Prégaldiny, C. Lallement, J.-M. Sallese, and F. Krummenacher, "Explicit compact models for symmetric double-gate MOSFETs including solution for small-geometry effects," *Solid State Electron.*, vol. 52, no. 1, pp. 99–106, Jan. 2008.

[13] G. Dessai and G. Gildenblat, "Solution space for the independent-gate asymmetric DGFET," *Solid State Electron.*, vol. 54, no. 4, pp. 382–384, Apr. 2010.

[14] D. Ward and R. Dutton, "A charge-oriented model for MOS transistor capacitances," *IEEE J. Solid-State Circuits*, vol. SSC-13, no. 5, pp. 703–708, Oct. 1978.

[15] *Mathematica Users' Manual*, Wolfram Res., Champaign, IL, 2010. [Online]. Available: www.wolfram.com

[16] A. Ortiz-Conde, F. J. Garcia-Sanchez, S. Malobabic, J. Muci, and R. Salazar, "Drain current and transconductance model for the undoped body asymmetric double-gate MOSFET," in *Proc. 8th Int. Conf. Solid-State Integr. Circuit Technol.*, Shanghai, China, Oct. 2006, pp. 1239–1242.

[17] *ATLAS Users' Manual*, Silvaco Int., Santa Clara, CA, 2010. [Online]. Available: www.silvaco.com

Pankaj Kumar Thakur received the B.Eng. degree in electrical and electronics engineering from Sri Chandrasekharendra Saraswathi Viswa Mahavidyalaya (Deemed University), Kanchipuram, India, in 2006 and the M.Eng. degree in microelectronics from the Birla Institute of Technology and Science, Pilani, India, in 2008. He is currently working toward the Ph.D. degree in the Nano Scale Device Research Laboratory, Centre for Electronics Design and Technology, Indian Institute of Science, Bangalore, India.

His research interests include the physics and modeling of semiconductor devices and designing analog mixed-signal RF circuits using advanced and post-CMOS devices.

Santanu Mahapatra (M'08–SM'10) received the B.E. degree in electronics and telecommunications from Jadavpur University, Kolkata, India, in 1999, the M.Tech. degree in electrical engineering, with specialization in microelectronics, from the Indian Institute of Technology (IIT), Kanpur, India, in 2001, and the Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology–Lausanne (EPFL), Lausanne, Switzerland, in 2005. His Ph.D. work was focused on the compact modeling of single-electron transistors and their hybridization with CMOS.

He joined the Centre for Electronics Design and Technology (CEDT), Indian Institute of Science (IISc), Bangalore, India, as an Assistant Professor in August 2005 and was promoted as an Associate Professor in September 2010 on an out-of-the-term basis. In 2006, he founded the Nano Scale Device Research Laboratory, CEDT, where his team is currently engaged in research on the compact modeling and simulation of emerging nanotechnologies and advanced CMOS devices. He has supervised many students for their Master's thesis and Ph.D. dissertation. He is the author or a coauthor of several papers published in international journals and refereed conference proceedings. He is also the author of the book *Hybrid CMOS Single Electron Transistor Device and Circuit Design* (Artech House, 2006). His current research interests include device reliability, multigate transistors, tunnel field-effect transistors, single-electron transistors, carbon nanoelectronics, and CMOS nanohybridization.

Prof. Mahapatra received the Best Paper Award at the International Semiconductor Conference (CAS), Romania, in 2003. He is also the recipient of an IBM Faculty Award in 2007, the Microsoft India Research Outstanding Faculty Award in 2007 and the Associateship of Indian Academy of Science in 2009.