A Short-Channel Common Double-Gate MOSFET Model Adapted to Gate Oxide Thickness Asymmetry

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***Abstract*— Existing compact models for common double-gate (CDG) MOSFETs are based on the fundamental assumption of having symmetric gate oxide thickness. In this paper, we demonstrate that using the unique quasi-linear relationship between the surface potentials, it is possible to develop compact model for CDG-MOSFETs without such approximation while preserving the mathematical complexity at the same level of the existing models. In the proposed model, the surface potential relationship is used to include the drain-induced barrier lowering, channel length modulation, velocity saturation, and quantum mechanical effect in the long-channel model and good agreement is observed with the technology computer aided design simulation results.**

***Index Terms*— Compact modeling, double gate (DG), MOSFET.**

I. Introduction

COMMON double-gate (CDG) MOSFETs have appeared as a replacement for bulk MOSFETs in sub-32-nm technology nodes [1], [2] due to their superior electrostatic integrity. Efficient compact models are required for successful utilization of such devices in integrated circuit design. Existing compact models for CDG-MOSFETs [3]–[7] are based on the fundamental assumption of having symmetric gate oxide thickness, as it greatly simplifies the model development process. However, the models could be generalized by considering the asymmetry between gate oxide thickness as there could be a possibility of having asymmetry between the gate oxide thickness due to process variations and uncertainties, which can affect device performance significantly. A similar problem is addressed in [8] for independent gate configuration with the back gate oxide thickness much higher than that of the front gate, electrostatic of which is quite different than that of the CDG device with comparable oxide thickness.

Using the single implicit equation-based Poisson solution and the unique quasi-linear relationship between the surface potentials, recently, we reported an efficient model for generic CDG MOSFET [9]–[11]. However, such effort was limited to long channel devices. In this paper, we extend this concept to model the drain-induced barrier lowering (DIBL), channel length modulation (CLM), velocity saturation, and quantum mechanical effects (QMEs), which are important for short-channel devices. The mathematical complexity of the proposed model appears to be at the same level of the existing models, and its accuracy is verified against the TCAD simulation [12] results.

Manuscript received March 20, 2014; revised May 12, 2014 and June 11, 2014; accepted June 13, 2014. Date of publication July 1, 2014; date of current version July 21, 2014. This work was supported by the Department of Science and Technology, Government of India, under the Ramanna Fellowship, under Grant SR/S3/EECE/0123/2011. The review of this paper was arranged by Editor Y. Momiyama.

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Digital Object Identifier 10.1109/TED.2014.2331191

II. Model Development

The conventions used in this paper are $t_{\mathrm{ox1(2)}}$ is the oxide thickness of the first (second) gate, t_{si} is the thickness of the silicon body, $C_{\mathrm{ox1(2)}}$ is the oxide capacitance per unit area of first (second) gate defined as $\epsilon_{\mathrm{ox}}/t_{\mathrm{ox1(2)}}$, ϵ_{si}, ϵ_{ox} are the permittivities of Si and SiO_2, respectively, q is the elementary charge, k is the Boltzmann constant, T is the absolute temperature, β is the inverse thermal voltage (q/kT), and n_i is the intrinsic carrier density, $B = 2\mathrm{qn}_i/\beta\epsilon_{\mathrm{si}}$, L is the channel length, W is the channel width, $\psi_{1(2)}$ are the Si/SiO_2 surface potentials at the first (second) gate, V is the electron quasi-Fermi potential (channel potential), E_g is the silicon bandgap, and μ is the effective mobility. The effective gate voltage with respect to source terminal is defined as $V_{\mathrm{gs}} = V_{\mathrm{gs,applied}} - \delta\phi$, where $V_{\mathrm{gs,applied}}$ is the voltage applied at gate terminals and $\delta\phi$ is the work function difference of the gate material. V_{ds} is the applied drain voltage with respect to source terminal. The inversion charge density at any point along the channel is denoted by Q_i, which is the sum of two components Q_{i1} and Q_{i2} expressed as $Q_{i1(2)} = C_{\mathrm{ox1(2)}}(V_{\mathrm{gs}} - \psi_{1(2)})$. In the following discussion, any variable with subscript s refers to its values at source end and subscript d refers to its value at drain end. The variable x denotes the direction along thickness of the channel with $x = \pm t_{\mathrm{si}}/2$ representing the front and back Si/SiO_2 interface. The variable y represents the direction along length of the channel, while $y = 0$ and L represent the source end and the drain end of the channel, respectively.

A. DIBL Model

In the presence of oxide thickness asymmetry, following the Suzuki's methodology [3], [13], the governing 2-D Poisson equation in subthreshold could be written as:

$$\frac{d^2\psi_1}{dy^2} + \frac{(V_{\mathrm{gs}} - \psi_1)}{\lambda^2} = 0 \tag{1}$$

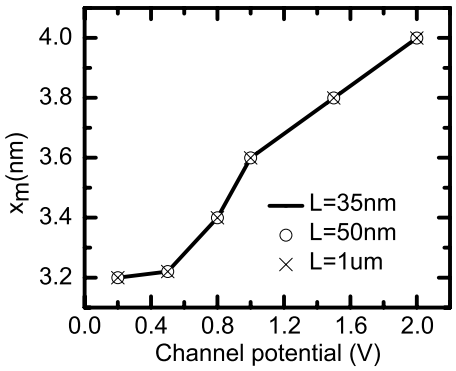

Fig. 1. Position of minimum potential x_m in the channel with variation in channel potential at $V_{gs} = 0.2$ V with $t_{si} = 10$ nm, $t_{ox1} = 1$ nm, $t_{ox2} = 2$ nm, and $W = 1$ μm.

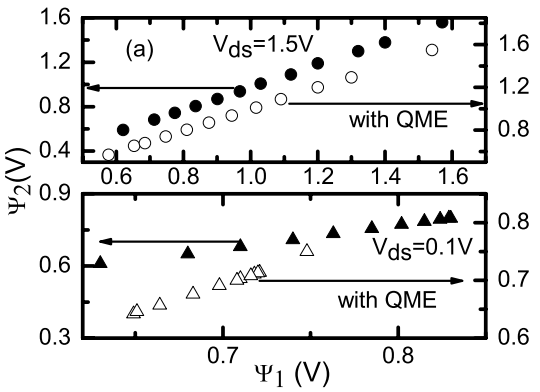

Fig. 2. Relationship between ψ_1 and ψ_2 with $t_{si} = 10$ nm, $t_{ox1} = 1$ nm, $t_{ox2} = 2$ nm, $L = 35$ nm, and $W = 1$ μm.

where λ defines the scale length, i.e., the limit to which the channel length of the device can be scaled for a particular structural parameter as follows:

$$\lambda = \sqrt{\frac{C_{si}}{C_{ox1}}\left(x_{m,av} + \frac{t_{si}}{2}\right)\left[t_{si} + \frac{C_{ox1}}{\epsilon_{si}}\frac{t_{si}^2}{2} - \frac{\frac{C_{ox1}}{\epsilon_{si}}\frac{t_{si}^3}{3}}{2\left(x_{m,av} + \frac{t_{si}}{2}\right)}\right]}. \tag{2}$$

Here, x_m denotes the position where vertical electric field $d\psi/dx$ is zero for a given channel potential and $x_{m,av}$ represents its average value. For short-channel devices, in subthreshold, current does not flow at surface but at x_m. In case of a symmetric device, $x_m = 0$ and λ leads to the same expression as in [13]. However, in the presence of oxide thickness asymmetry, finding x_m is not trivial. From TCAD simulation, we observe (Fig. 1) that in the case of asymmetric device, for a given bias condition: 1) x_m changes from source to drain end and 2) its value remains almost invariant at a particular channel potential, while the channel length scales down keeping the other parameters constant. Therefore, we can conclude that x_m calculated from the long channel 1-D Poisson equation [9] can be used for short-channel devices. Now, linearizing the right-hand side (RHS) of the Poisson equation [9, eq. (1)] and then solving it rigorously with the same boundary conditions, the value of x_m in the subthreshold could be obtained as

$$x_m = \left(\frac{\epsilon_{si}}{qn_i\beta}\right)^{\frac{1}{2}}\frac{1}{2}\log\left(\frac{A_1}{B_1}\right) \tag{3}$$

where

$$A_1 = \frac{X_{s1}W_1(1+\beta(V+V_{gs}))+X_{c1}(W_2 - VW_3 + W_3V_{gs})}{\beta\left(W_1X_{s2}+W_2C_{ox1}X_{a2}+C_{ox2}W_2X_{a2}+X_{s2}\beta\epsilon_{si}qn_i\right)} \tag{4}$$

$$B_1 = \frac{X_{s1}W_1(1+\beta(V-V_{gs}))+X_{c1}(W_2 + V_{gs}W_3 + W_3V)}{\beta\left(W_1X_{s2}+W_2C_{ox1}X_{a2}+C_{ox2}W_2X_{a2}+X_{s2}\beta\epsilon_{si}qn_i\right)} \tag{5}$$

with $W_1 = C_{ox1}C_{ox2}$, $W_2 = \epsilon_{si}\beta\sqrt{B/2}$, $W_3 = \beta^2\epsilon_{si}\sqrt{B/2}$, $X_{s1} = (X_1 - 1/X_1)$, $X_{c1} = (C_{ox1}X_1 + C_{ox2}/X_1)$, $X_{s2} = (X_2 - 1/X_2)$, $X_{a2} = (X_2 + 1/X_2)$, $X_1 = e^{t_{si}/2\sqrt{\beta n_i q/\epsilon_{si}}}$, and $X_2 = e^{t_{si}\sqrt{\beta n_i q/\epsilon_{si}}}$. Now, as x_m is a function of channel potential, to calculate the potential at virtual cathode (ψ_{min}), we use an average value of it. Though there could be several options for calculating $x_{m,av}$, in this paper, we find it as $x_{m,av} = x_m$@source as the virtual cathode moves toward source as V_{ds} increases. Following [13], we solve (1) to obtain:

$$\psi_{min} = V_{gs} + \frac{(V_{ds} + E_g + V_{gs})\left[e^{\frac{L}{2\lambda}} - e^{-\frac{L}{2\lambda}}\right]}{\left[e^{\frac{L}{\lambda}} - e^{-\frac{L}{\lambda}}\right]}. \tag{6}$$

We then model DIBL using precorrection technique by changing the actual gate voltage to effective gate voltage as $V_{gs,eff} = V_{gs} + \Delta V_g$, where $\Delta V_g = \psi_{min} - V_{gs}$.

B. Velocity Saturation Effect

To model velocity saturation effect, we use the lateral electric field dependence mobility expression in drain current as [14]

$$I_d = \frac{\mu}{\left[1 + \left(\frac{\mu}{v_{sat}}\frac{dV}{dy}\right)^2\right]^{1/2}} W Q_i \frac{dV}{dy} \tag{7}$$

where v_{sat} is saturation velocity and μ is the low field electron mobility, which is taken as constant here. μ could also be made a function of vertical electric field [15]

$$\underbrace{I_d \int_0^L \left[1 + \left(\frac{\mu}{v_{sat}}\frac{dV}{dy}\right)^2\right]^{1/2} dy}_{LH} = \int_0^{V_{ds}} \mu W Q_i dV. \tag{8}$$

Here, the RHS expression is the same as that for long-channel device. To evaluate the LHS expression, we assume that for a given bias condition, the surface potentials along the undoped channel hold a linear relationship [10]. As observed in Fig. 2, this assumption remains valid even in the case of short-channel devices in the presence of velocity saturation and QMEs. Using dV/dQ_i [11, eq. (3)] and dQ_i/dy [10], we get

$$LH = \int_{Q_{is}}^{Q_{id}} \left[I_{n1}^2 + \frac{I_{n2}^2}{E_c^2(1+m_1)^2}\right]^{1/2} dQ_i \tag{9}$$

with

$$I_{n1} = \left\{\frac{2\alpha_1 L Q_1 + \gamma_1 L(1+m_1)}{(1+m_1)^2}\right\}$$

$$I_{n2} = \left\{\frac{1}{C_{\rm ox1}} + \frac{[2{\rm nQ}_1 + p_1(1+m_1)](1+m_1)}{\beta[nQ_1{}^2 + p_1(1+m_1)Q_1 + q_1(1+m_1)^2]}\right\}.$$

$Q_1 = (Q_i - c_1)$, $E_c = \upsilon_{\rm sat}/\mu$ is the critical electric field, $n = 1/\epsilon_{\rm si}^2$, and $p_1 = -s_1$, $q_1 = -k_1$, α_1, γ_1, m_1, and c_1 are the linearization coefficients of the surface potential evaluated in the same way as in [10].

A direct solution of (8) is difficult to find. It is observed through inspection that the behavior of I_{n2}^2 is a quadratic function of inversion charge over a varied range of bias conditions, and so we approximate I_{n2}^2 as

$$I_{n2}^2 \simeq N_1(Q_1) = E_1 Q_1^2 + F_1 Q_1 + G_1 \tag{10}$$

with

$$E_1 = \frac{\zeta_1 - \zeta_2}{\zeta_3 - \zeta_4}$$

$$F_1 = \frac{(N_1(Q_{1s}) - N_1(Q_{1m})) - \left(E_1\left(Q_{1s}^2 - Q_{1m}^2\right)\right)}{(Q_{1s} - Q_{1m})}$$

$$G_1 = N_1(Q_{1m}) - \left(E_1 Q_{1m}^2\right) - (F_1 Q_{1m})$$

where

$$\zeta_1 = \{(N_1(Q_{1s}) - N_1(Q_{1m}))(Q_{11d} - Q_{1m})\}$$

$$\zeta_2 = \{(N_1(Q_{11d}) - N_1(Q_{1m}))(Q_{1s} - Q_{1m})\}$$

$$\zeta_3 = \left(Q_{1s}^2 - Q_{1m}^2\right)(Q_{1d} - Q_{1m})$$

$$\zeta_4 = \left(Q_{11d}^2 - Q_{1m}^2\right)(Q_{1s} - Q_{1m})$$

$$Q_{1s} = Q_{is} - c_1, \quad Q_{1d} = Q_{id} - c_1$$

$$Q_{1m} = q_{f1}(Q_{1s} + Q_{1d}), \quad Q_{11d} = q_{f2}(Q_{1s} + Q_{1d}).$$

Further evaluating left-hand side (LHS) and equating LHS with RHS, we get the drain current expression as

$$I_d = -\frac{\mu W[F_s - F_d](1+m_1)}{[\Theta_1 + \Theta_2]_{Q_{1s}}^{Q_{1d}}} \tag{11}$$

with $\Theta_1 = J_1 + 2O_1Q_1/4O_1\sqrt{\varpi}$, $\varpi = O_1Q_1^2 + J_1Q_1 + Z_1$

$$\Theta_2 = \frac{4O_1Z_1 - J_1^2}{8O_1^{3/2}} \log\left(2O_1Q_1 + J_1 + 2\sqrt{O_1\varpi}\right)$$

where $O_1 = 4\alpha_1^2L^2/(1+m_1^2) + E_1/E_c^2$, $J_1 = 4\alpha_1\gamma_1L^2/(1+m_1) + F_1/E_c^2$, $Z_1 = \gamma_1^2L^2 + G_1/E_c^2$, and F_s and F_d are the same as in [10].

Since, in velocity saturation regime, the drain current becomes invariant with bias condition, we calculate the saturation voltage $V_{\rm sat1(2)}$ through $dI_d/{\rm dV} = 0$. That is, when $V_{\rm ds}$ is less than saturation voltage, the voltage at the drain side will be $V_{\rm ds}$; otherwise, it will be saturation voltage, $V_{\rm sat1(2)}$. To make this transition from drain voltage to saturation voltage smooth, we use the following function [7]:

$$V_{\rm ds1(2),eff} = V_{\rm ds}\left(1 + \left(\frac{V_{\rm ds}}{V_{\rm sat1(2)}}\right)^f\right)^{-1/f}. \tag{12}$$

C. Channel Length Modulation

Evaluating (1) in the same way as [7], we get

$$\Delta L_{1(2)} = \frac{\lambda log\left(\varphi_d + \sqrt{\varphi_d^2 - \left(\varphi_{\rm sat1(2)}^2 - \frac{2\upsilon_{\rm sat}\lambda}{\mu}\right)^2}\right)}{\varphi_{\rm sat1(2)} + \frac{2\upsilon_{\rm sat}\lambda}{\mu}} \tag{13}$$

where $\varphi_{\rm sat1(2)} = V_{\rm gs} - \psi_{\rm sat1(2)}$ and $\psi_{\rm sat1(2)} = V_{\rm ds1(2),eff} + (E_g/2)$.

Since, in an asymmetric CDG MOSFET, the saturation voltage $V_{\rm sat1(2)}$ and CLM factor $\Delta L_{1(2)}$ are different for both channels, we need to evaluate the drain current independently at both surfaces. Evaluating the drain current across the front surface in the same way as in (8) and using the relation [11, eq. (3)] and ${\rm dQ}_{i1(2)}/{\rm dy}$ [10, eq. (14)], we get

$$I_{d1(2)}\left[\chi 1_{1(2)}^2 + \frac{1}{E_c^2}\chi 2_{1(2)}^2\right]^{1/2} {\rm dQ}_{i1(2)} = \mu W Q_{i1(2)} dV \tag{14}$$

where

$$\chi 1_{1(2)} = \left\{2\alpha_{1(2)}\Delta L_{1(2)}Q_{i1(2)} + \gamma_{1(2)}\Delta L_{1(2)}\right\}$$

$$\chi 2_{1(2)} = \left\{-\frac{1}{C_{\rm ox1(2)}} - \frac{[2{\rm nQ}_{i1(2)} + p_{1(2)}]}{\beta\left[nQ_{i1(2)}^2 + p_{1(2)}Q_{i1(2)} + q_{1(2)}\right]}\right\}$$

and $n = 1/\epsilon_{\rm si}^2$, and $p_{1(2)} = -s_{1(2)}$ and $q_{1(2)} = -k_{1(2)}$ are the linearization coefficients of the surface potential evaluated in the same way as in [10]. Similar to (8), the direct solution of (14) is also not possible, and so we approximate

$$\chi 2_{1(2)}^2 \simeq \vartheta_{1(2)}(Q_{i1(2)}) = \left(R_{1(2)}Q_{i1(2)}^2 + T_{1(2)}Q_{i1(2)} + V_{1(2)}\right)$$

where

$$R_{1(2)} = \frac{\delta 1_{1(2)} - \delta 2_{1(2)}}{\delta 3_{1(2)} - \delta 4_{1(2)}}$$

$$T_{1(2)} = \frac{\left(\vartheta_{1(2)}(Q_{i1(2)s}) - \vartheta_{1(2)}(Q_{i1(2)m})\right) - \left(R_{1(2)}Q_{\rm sqr}\right)}{\left(Q_{i1(2)s} - Q_{i1(2)m}\right)}$$

$$V_{1(2)} = \vartheta_{1(2)}(Q_{i1(2)m}) - \left(R_{1(2)}Q_{i1(2)m}^2\right) - \left(T_{1(2)}Q_{i1(2)m}\right)$$

$$\delta 1_{1(2)} = \left\{(\vartheta_{1(2)}(Q_{i1(2)s}) - \vartheta_{1(2)}(Q_{i1(2)m})) \times (Q_{i11(2)d} - Q_{i1(2)m})\right\}$$

$$\delta 2_{1(2)} = \left\{(\vartheta_{1(2)}(Q_{i11(2)d}) - \vartheta_{1(2)}(Q_{i1(2)m})) \times (Q_{i1(2)s} - Q_{i1(2)m})\right\}$$

$$\delta 3_{1(2)} = \left(Q_{i1(2)s}^2 - Q_{i1(2)m}^2\right)(Q_{i11(2)d} - Q_{i1(2)m})$$

$$\delta 4_{1(2)} = \left(Q_{i11(2)d}^2 - Q_{i1(2)m}^2\right)(Q_{i1(2)s} - Q_{i1(2)m}).$$

$Q_{\rm sqr} = \left(Q_{i1(2)s}^2 - Q_{i1(2)m}^2\right)$, $Q_{i1(2)s} = Q_{i1(2)s}$, $Q_{i1(2)d} = Q_{i1(2)d}$, $Q_{i1(2)m} = q_{f3}(Q_{i1(2)s} + Q_{i1(2)d})$, and $Q_{i11(2)d} = q_{f4}(Q_{i1(2)s} + Q_{i1(2)d})$.

Further evaluating (14) with the above approximation, we get

$$I_{d1(2)} = \frac{\mu W[F_{s1(2)} - F_{d1(2)}]}{\left[\Theta 1_{1(2)} + \Theta 2_{1(2)}\right]_{Q_{i1(2)s}}^{Q_{i1(2)d}}} \tag{15}$$

where

$$\Theta 1_{1(2)} = \frac{J_{i1(2)} + 2O_{i1(2)}Q_{i1(2)}}{4O_{i1(2)}}\sqrt{\varpi_{1(2)}}$$

$$\Theta 2_{1(2)} = \frac{4O_{i1(2)}Z_{i1(2)} - J_{i1(2)}^2}{8O_{i1(2)}^{3/2}}\log(\Lambda_{1(2)})$$

$$F_{s1(2)} = \frac{Q_{i1(2)s}^2}{C_{\text{ox1(2)}}} + \frac{2}{\beta}Q_{i1(2)s} + \frac{1}{2}\epsilon_{\text{si}}t_{\text{si}}(s_{1(2)}Q_{i1(2)s} + k_{1(2)})$$

$$F_{d1(2)} = \frac{Q_{i1(2)d}^2}{C_{\text{ox1(2)}}} + \frac{2}{\beta}Q_{i1(2)d} + \frac{1}{2}\epsilon_{\text{si}}t_{\text{si}}(s_{1(2)}Q_{i1(2)d} + k_{1(2)})$$

$$\Lambda_{1(2)} = 2O_{i1(2)}Q_{i1(2)} + J_{i1(2)} + 2\sqrt{O_{i1(2)}\varpi_{1(2)}}$$

$$\varpi_{1(2)} = O_{i1(2)}Q_{i1(2)}^2 + J_{i1(2)}Q_{i1(2)} + Z_{i1(2)}$$

$$O_{i1(2)} = 4\alpha_{1(2)}^2\Delta L_{1(2)}^2 + \frac{R_{1(2)}}{E_c^2}$$

$$J_{i1(2)} = 4\alpha_{1(2)}\gamma_{1(2)}\Delta L_{1(2)}^2 + \frac{T_{1(2)}}{E_c^2}$$

and

$$Z_{i1(2)} = \gamma_{1(2)}^2\Delta L_{1(2)}^2 + \frac{V_{1(2)}}{E_c^2}.$$

Finally, the total drain current across the device is given as

$$I_d = I_{d1} + I_{d2}. \tag{16}$$

D. Quantum Mechanical Effect

We include QME in our model through two approaches: 1) calculating threshold voltage shift due to QME and including it in model by effective gate voltage and 2) calculating the effective oxide thickness due to shift in inversion charge centroid.

1) Threshold Voltage Shift Model: In an undoped channel, the inversion charge [16], [17] is expressed as

$$Q_{i,\text{qm}} = \frac{qKT}{\pi\hbar^2}\sum_i\sum_j g_i m_i \log\left(1 + e^{-\left(E_{i,j} + \frac{E_g}{2} - \psi\right)\beta}\right) \tag{17}$$

where g_i stands for the degeneracy factor, m_i stands for the density of states effective mass of an electron, E_g is the energy bandgap, and $E_{i,j}$ stands for the energy level of the jth subband in ith valley. The unknown factors here are $E_{i,j}$ and ψ. To find the potential profile, we need to solve the 2-D Poisson equation. Solving Laplace equation with the following boundary condition: $d\psi/dx\ |_{x=-\text{tsi}/2} = -C_{\text{ox1}}/\epsilon_{\text{si}}(V_{\text{gs}} - \psi_1)$, $\psi(-t_{\text{si}}/2 - t_{\text{ox1}}, y) = V_{\text{gs}}$, $\psi(t_{\text{si}}/2 + t_{\text{ox2}}, y) = V_{\text{gs}}$.

We get the solution

$$\psi(x, y) = C_{q0} + C_{q1}x + C_{q2}x^2 \tag{18}$$

where

$$C_{q2} = \frac{\frac{C_{\text{ox1}}}{\epsilon_{\text{si}}}(V_{\text{gs}} - \psi_1)(-t_{\text{si}} - t_{\text{ox1}} - t_{\text{ox2}})}{\varrho}$$

$$C_{q1} = C_{q2}t_{\text{si}} - \frac{C_{\text{ox1}}}{\epsilon_{\text{si}}}(V_{\text{gs}} - \psi_1)$$

$$C_{q0} = V_{\text{gs}} - \left(\frac{t_{\text{si}}}{2} + t_{\text{ox1}}\right)\left(\frac{C_{\text{ox1}}}{\epsilon_{\text{si}}}(V_{\text{gs}} - \psi_1) - C_{q2}\left(\frac{t_{\text{si}}}{2} - t_{\text{ox1}}\right)\right)$$

$$\varrho = \left(-\frac{t_{\text{si}}}{2} - t_{\text{ox1}}\right)\left(\frac{t_{\text{si}}}{2} - t_{\text{ox1}}\right) - \left(\frac{t_{\text{si}}}{2} + t_{\text{ox2}}\right)\left(\frac{3t_{\text{si}}}{2} + t_{\text{ox2}}\right).$$

ψ_1 is unknown here. We evaluate ψ_1 in a similar way as done in [3] to get

$$\psi_1 = V_{\text{gs}} + U_1\sinh\left(\frac{y_m}{Q_{12}}\right) + U_2\cosh\left(\frac{y_m}{Q_{12}}\right) \tag{19}$$

where

$$Q_{12} = \sqrt{\varrho\left(\frac{Q_{11}^2 C_{\text{si}}}{2C_{\text{ox1}}(-t_{\text{si}} - t_{\text{ox1}} - t_{\text{ox2}})}\right)}$$

$$Q_{11} = \sqrt{\frac{C_{\text{ox1}}}{\epsilon_{\text{si}}}\left[H_1 + H_2\left\{\frac{-(t_{\text{si}} + t_{\text{ox1}} + t_{\text{ox2}})}{\varrho}\right\}\right]}$$

$$H_1 = \left(\frac{t_{\text{si}}}{2} + t_{\text{ox1}}\right)t_{\text{si}}, \quad U_1 = V_{\text{gs}} - \frac{E_g}{2}$$

$$H_2\left\{\left(-\frac{t_{\text{si}}}{2} - t_{\text{ox1}}\right)\left(\frac{t_{\text{si}}}{2} - t_{\text{ox1}}\right)t_{\text{si}} - \frac{t_{\text{si}}^3}{12}\right\}$$

$$U_2 = \frac{V_{\text{gs}} - U_1\cosh\left(\frac{L}{Q_{12}}\right) - \frac{E_g}{2} - V_{\text{ds}}}{\sinh\left(\frac{L}{Q_{12}}\right)}.$$

Now, to find $E_{i,j}$, we need to solve the Schrodinger equation. In a CDG MOSFET, the quantum well comprises front gate oxide barrier, back gate oxide barrier, and the conduction band of the silicon channel. Therefore, the energy quantization in a CDG MOSFET is due to both structural (silicon thickness) and electrical confinement (slope of conduction band). It is observed that the potential profile in a long-channel CDG MOSFET can be approximated as an infinite square well [18], and to include the short-channel term, we use perturbation technique. Applying first-order perturbation to the 2-D potential term of an infinite square well, we get

$$E_j = \frac{j^2\hbar^2\pi^2}{2mt_{\text{si}}^2} + \left(\frac{C_{q2}t_{\text{si}}^2}{12} + (-1)^j\frac{C_{q2}t_{\text{si}}^2}{2\pi^2}\right)q. \tag{20}$$

Taking the definition of threshold voltage to be a voltage at which the inversion charge reaches a constant value [17] of $Q_{i1,\text{qm}} = kT/qC_{\text{ox1}}$ and $Q_{i2,\text{qm}} = kT/qC_{\text{ox2}}$, we calculate the respective gate threshold voltage. Finally, to calculate the respective effective gate voltage, we use an average threshold voltage, $V_t = (V_{t1} - V_{t2})/5$. Using the relation $V_{\text{gs,qeff}} = V_{\text{gs}} + V_t$, we calculate the respective effective gate voltage.

2) Effective Oxide Thickness Model: The inversion charge depth $\text{inv}_{\text{depth}}$ in a CDG MOSFET is calculated using the same expression as in [19]. The respective location of the inversion charge in the channel across both surfaces is given as $\text{inv1} = (-t_{\text{si}}/2) - \text{inv}_{\text{depth}}$, $\text{inv2} = (+t_{\text{si}}/2) - \text{inv}_{\text{depth}}$.

From this, we calculate the respective inversion charge centroid, $\text{inv1(2)}_{\text{centroid}}$ as

$$\text{inv1(2)}_{\text{centroid}} = \int_{-\frac{t_{\text{si}}}{2}}^{\text{inv1(2)}} \psi^2 \text{d}x. \tag{21}$$

The quantum mechanical gate oxide capacitance is given as

$$C_{\text{ox1(2),eff}} = \frac{C_{\text{ox1(2)}}}{1 + \frac{C_{\text{ox1(2)}}\text{inv1(2)}_{\text{centroid}}}{\epsilon_{\text{si}}}}. \tag{22}$$

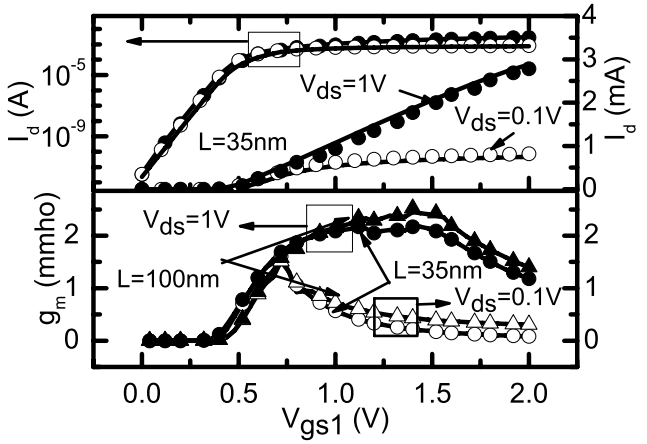

Fig. 3. Drain current versus gate voltage characteristics and transconductance behavior as obtained from the TCAD simulation (symbol) and the proposed model (line).

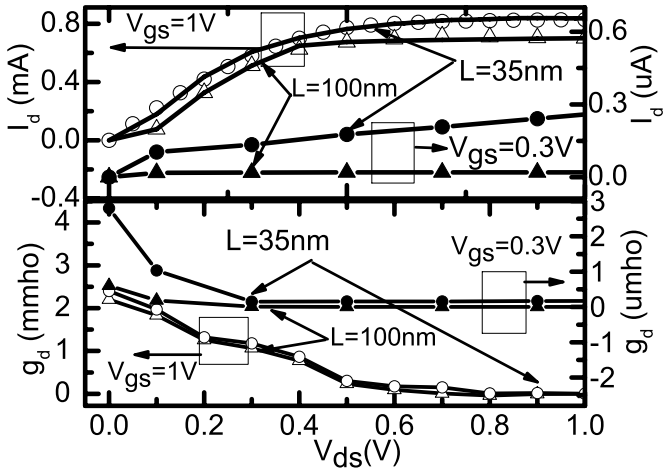

Fig. 4. Drain current versus drain voltage plot and conductance characteristics as obtained from the TCAD simulation (symbol) and the proposed model (line).

The respective oxide thickness can be calculated as $t_{\mathrm{ox1(2),eff}} = \epsilon_{\mathrm{ox}}/C_{\mathrm{ox1(2),eff}}$. In a CDG MOSFET, when the gate voltage is low, the carrier quantization is basically dominated by structural confinement. It is only when the gate voltage is higher than the threshold voltage, both structural and electrical confinement starts affecting the quantization.

All effects are thus captured in the form of effective gate voltage and capacitances. The IVE [9] is solved with these effective values to obtain the surface potentials.

III. Results and Discussion

We have validated our model against the 2-D TCAD simulation results [12] for devices having gate oxide thickness asymmetry: $t_{\mathrm{ox1}} = 1$ nm, $t_{\mathrm{ox2}} = 1.5$ nm, $t_{\mathrm{si}} = 10$ nm, and $W = 1$ μm for different channel lengths, as shown in Figs. 3–6. The minimum channel length is taken to be 35 nm according to the scale length criteria $L/2\lambda > 3$. The value of λ (grounded source) changes from 4.84 to 5.46 nm as the back gate oxide thickness increases from 1 to 2 nm. We use Caughey-Thomas velocity saturation model in TCAD. For the TCAD simulation of QME, we need to include a particular

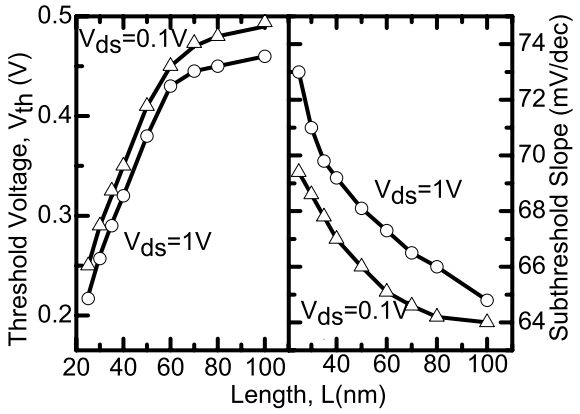

Fig. 5. Threshold voltage (extracted by linear extrapolation method) rolloff and subthreshold slope with decrease in channel length predicted from the TCAD simulation (symbol) and the proposed model (line).

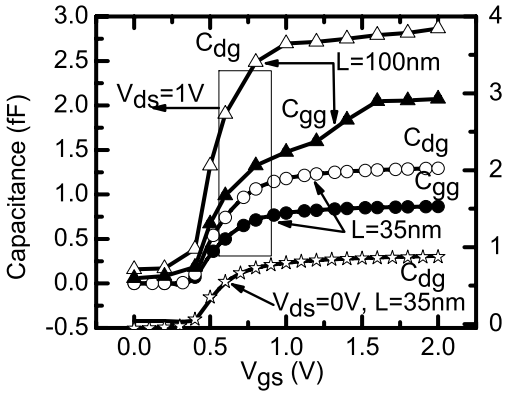

Fig. 6. Transcapacitance plot from the TCAD simulation (symbol) and the proposed model (line) with variation in gate voltage from 0 to 2 V.

set of model (SCHRO) that cannot be merged with velocity saturation model. Fig. 3 shows the variation in drain current and transconductance characteristics as a function of gate voltage. Fig. 4 shows the change in drain current and output conductance characteristics as a function of drain bias. The threshold voltage rolloff and subthreshold slope as extracted from the TCAD simulation and the proposed model is shown in Fig. 5. We find that the proposed model works well till $L \simeq 4\lambda$ (which is 25 nm and 33 nm for $t_{\mathrm{si}} = 10$ nm and 20 nm, respectively, with $t_{\mathrm{ox1}} = 1$ nm and $t_{\mathrm{ox2}} = 1.5$ nm) provided that the ballistic transport is insignificant. Fig. 6 shows the transcapacitance (C_{dg} and C_{gg}) characteristics at different bias conditions. Though the Ward-Dutton partition theory is not applicable for velocity saturation Ananda, we can minimize the error by properly tuning the model parameters. Fig. 7 shows the variation in drain current with variation in gate voltage with inclusion of QME. In all these cases, the proposed model is in excellent agreement with the TCAD simulation results. We have also calibrated the model for devices having: $t_{\mathrm{ox1}} = 1$ nm, $t_{\mathrm{ox2}} = 2$ nm, $t_{\mathrm{ox1}} = 1$ nm, $t_{\mathrm{ox2}} = 1.5$ nm, $t_{\mathrm{ox1}} = 1$ nm, and $t_{\mathrm{ox2}} = 1$ nm against TCAD simulation. The calibrated values for different model parameters are given in Table I. One can see that the mathematical complexity and the number of model parameters used in the proposed models

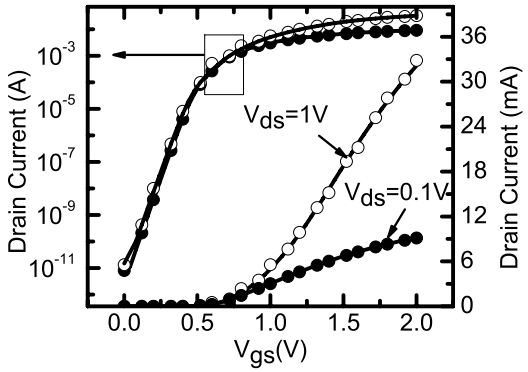

Fig. 7. Effect of QME on the drain current versus gate voltage characteristics.

TABLE I
CALIBRATED MODEL PARAMETERS

parameters	Device 1(1:2)	Device 2(1:1.5)	Device 3(1:1)
q_{f1}	0.85	0.85	0.85
q_{f2}	0.25	0.25	0.25
f	1.2	1.2	1.2
q_{f3}	0.61	0.78	0.98
q_{f4}	0.60	0.62	0.72
y_m	L/12	L/12	L/12

is comparable with the existing models [3], [6], [7] that are based on the symmetric t_{ox} approximations.

IV. CONCLUSION

Using the unique quasi-linear relationship between the surface potentials, we propose a compact model for CDG MOSFET, which is adapted to the gate oxide thickness asymmetry, and the mathematical complexity is in the same level of the existing models. The model includes several small geometry effects and is found to be in good agreement with the TCAD simulation results.

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