Improvements in Efficiency of Surface Potential Computation for Independent DG MOSFET

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***Abstract*—A robust numerical solution of the input voltage equations (IVEs) for the independent-double-gate metal–oxide–semiconductor field-effect transistor requires root bracketing methods (RBMs) instead of the commonly used Newton–Raphson (NR) technique due to the presence of nonremovable discontinuity and singularity. In this brief, we do an exhaustive study of the different RBMs available in the literature and propose a single derivative-free RBM that could be applied to both trigonometric and hyperbolic IVEs and offers faster convergence than the earlier proposed hybrid NR–Ridders algorithm. We also propose some adjustments to the solution space for the trigonometric IVE that leads to a further reduction of the computation time. The improvement of computational efficiency is demonstrated to be about 60% for trigonometric IVE and about 15% for hyperbolic IVE, by implementing the proposed algorithm in a commercial circuit simulator through the Verilog-A interface and simulating a variety of circuit blocks such as ring oscillator, ripple adder, and twisted ring counter.**

***Index Terms*—Circuit simulation, compact modeling, independent-double-gate metal–oxide–semiconductor field-effect transistor (IDG MOSFET).**

I. Introduction

An efficient solution for the implicit input voltage equations (IVEs) [1] for independent-double-gate (IDG) MOSFETs is a nontrivial task due to the presence of discontinuity in the IVEs at the G-zero point (where it changes from trigonometric to hyperbolic and vice versa) and the nonremovable singularities in trigonometric IVEs. The commonly used Newton–Raphson (NR) method fails to provide guaranteed and rapid convergence under such conditions. Further, the NR method is nonoptimal when the derivative computation is lengthy or when the initial guess for the root is not obvious. This necessitates the use of derivative-free root bracketing methods (RBMs) to solve these IVEs. Recently, a unique algorithm to solve the IVEs was proposed by combining the NR method and the Ridders root-finding method [2]. The hyperbolic IVE was solved using the NR method backed up by the Ridders method [3], whereas the trigonometric-mode IVE was solved using the Ridders method alone, with the aim of achieving assured convergence under any bias condition. In this brief, we propose a new RBM that completely eliminates the need for derivative computation. The choice of a single root-finding algorithm, to solve both the trigonometric and hyperbolic IVEs, also simplifies the overall surface potential calculation procedure. The performance of several RBMs [4]–[8] reported in the literature was studied, and the LZ*4* [8] algorithm was chosen to replace the hybrid NR–Ridders technique. A further speedup of 12%–15% in the computation time is achieved for the trigonometric IVE solution by replacing the exact upper bound for the solution space described in [2], by a simplified approximate bound with an improved initial guess. The proposed IVE solution technique is implemented in a commercial circuit simulator, using the Verilog-A interface. By simulating a variety of circuit blocks such as the 51-stage ring oscillator, the 8-bit ripple adder, and the 8-bit twisted ring counter, it is shown to be more efficient (60% for trigonometric IVE and 15% for hyperbolic IVE) than the previously reported technique.

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II. Algorithm Development

A. Study of RBMs

The conventions used in this brief are as follows: $C_{\mathrm{ox1(2)}}$ is the oxide capacitance per unit area of the first (second)-gate defined as $\epsilon_{\mathrm{ox}}/t_{\mathrm{ox1(2)}}$, $\varepsilon_{\mathrm{si}}$ and $\varepsilon_{\mathrm{ox}}$ are the permittivities, and t_{si} and t_{ox} are the thicknesses of Si and SiO_2, respectively. q is the elementary charge, β is the inverse thermal voltage, n_i is the intrinsic carrier density, V is the electron quasi-Fermi potential (channel potential), $\psi_{1(2)}$ is the Si/SiO_2 interface potential at the first (second) gate, and $V_{gs1(2)}$ is the effective front (back)-gate voltage, i.e., $V_{gs1(2)} = V_{gs1(2)\mathrm{applied}} - \Delta\phi_{1(2)}$, where $\Delta\phi_{1(2)}$ is the work function difference at the respective gates.

The numerical efficiency of any iterative root finding method is decided by its rate of convergence (ROC) and the number of function (NOF) or derivative evaluations required at each iteration step. Table I shows these parameters for the algorithm used in [2] and for the set of five algorithms, which demonstrated a superior efficiency among the several RBMs considered for study. Fig. 1 depicts the total root computation time for solving the trigonometric IVE, normalized with respect to the Ridders algorithm, for the five root finding algorithms mentioned in Table I. The computation time is recorded after implementing the algorithm in "C" using the GNU compiler collection version

TABLE I
COMPARISON OF DIFFERENT RBMS

Algorithm	*ROC*	*NOF / iteration*
Ridders [3]	2	2
Brent [4]	1.618	1
Dekker (Algo. M in [5])	1.626	1
Alefeld-Potra (Algo. 4.2 in [6])	4.646	3 or 4
LZ3 [7]	1.839	1
LZ4 [8]	<3	1

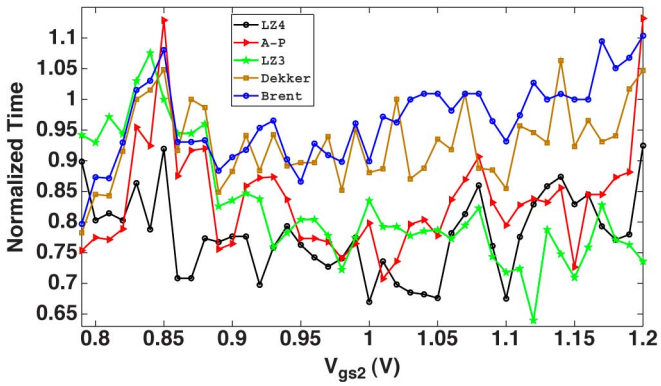

Fig. 1. Comparison of normalized root computation time for different algorithms to solve the trigonometric IVE using $\psi_{1\text{limit}}$ as the upper bound. $V_{gs1} = 1.2$ V and $V = 0.4$ V. V_{gs2} is swept from $V_{gs2\text{crit}} = 0.783$ V to 1.2 V. The device parameters are $t_{\text{ox1}} = 2$ nm, $t_{\text{ox2}} = 1$ nm, and $t_{\text{si}} = 25$ nm. Here, "A-P" refers to algorithm-4.2 in [6], and "Dekker" refers to algorithm-M in [5].

4.1.2 20080704 (Red Hat 4.1.2-50). One can see that all the considered algorithms perform better than the Ridders method, with LZ4 outperforming the rest. The superior performance of this algorithm can be attributed to the use of a higher order numerical method in its basic iterative process while retaining the root bracketing property and speeding up the convergence through occasional bisection steps. The high-order numerical method is realized using an approximating function based on Taylor polynomials where all the necessary derivative terms are replaced by their divided difference approximations using only the function values [8]. It should be noted in Fig. 1 that $\psi_{1\text{limit}}$ [2] is used as the upper bound for the solution space of the trigonometric IVE. A further reduction in the computation time could be achieved by adjusting this limit, as discussed in the next section. In the case of the hyperbolic IVE, the performance of the Alefeld–Potra, Brent and LZ4 algorithms is found to be similar and better than the hybrid NR–Ridders technique. Hence, we choose to use the LZ4 algorithm to solve both the trigonometric and hyperbolic IVEs.

B. Adjustment of the Upper Bound for the Trigonometric IVE

A solution using a RBM requires determination of the bounds for the root. As discussed in [2], the exact upper limit $\psi_{1\text{limit}}$ for the trigonometric solution space is obtained by solving the following implicit equation:

$$f_{\text{lt\_trig1}} = \pi - \left[\frac{\sqrt{G}\beta t_{\text{si}}}{2} + \sin^{-1}\left(\frac{\sqrt{G}}{\sqrt{Be^{\beta(\psi_1 - V)}}}\right)\right] = 0 \tag{1}$$

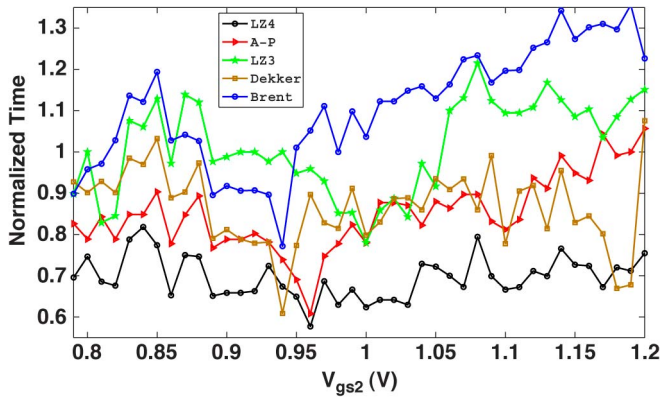

Fig. 2. Comparison of normalized root computation time for different algorithms to solve the trigonometric IVE using $\psi_{1\chi}$ as the upper bound. $V_{gs1} = 1.2$ V and $V = 0.4$ V. V_{gs2} is swept from $V_{gs2\text{crit}} = 0.783$ V to 1.2 V. The device parameters are $t_{\text{ox1}} = 2$ nm, $t_{\text{ox2}} = 1$ nm, and $t_{\text{si}} = 25$ nm. Here, "A-P" refers to algorithm-4.2 in [6], and "Dekker" refers to algorithm-M in [5].

where $G = -[(C_{\text{ox1}}/\epsilon_{\text{si}})(V_{gs1} - \psi_1)]^2 + Be^{\beta(\psi_1 - V)}$ and $B = 2qn_i/\beta\epsilon_{\text{si}}$. Since G can change signs, the hybrid NR–Ridders algorithm was employed to solve (1). For this process, $\psi_{1\chi}$ was used as the upper bound for the root, which is obtained by solving [2, Eq. (12)] using Halley's method. This two-step procedure for determining $\psi_{1\text{limit}}$ is extremely cumbersome and hence inefficient. This accounts for an overhead up to 30% in the trigonometric IVE solution process. Although the first step, i.e., the calculation of $\psi_{1\chi}$ is relatively fast, $\psi_{1\text{limit}}$ computation is time consuming. This procedure is simplified using $\psi_{1\chi}$ itself as the upper bound instead of $\psi_{1\text{limit}}$ while solving the trigonometric IVE. For ψ_1 lying in the range of $\psi_{1\text{limit}}$ to $\psi_{1\chi}$, the trigonometric function can have a discontinuity and a sign change. To avoid this, θ is limited to π for values of ψ_1 beyond $\psi_{1\text{limit}}$ so as to ensure the continuity of the function until $\psi_{1\chi}$. This modification also retains the sign of the function seen at $\psi_{1\text{limit}}$ until $\psi_{1\chi}$. Hence, the simplified upper bound $\psi_{1\chi}$ can be effectively used with any RBM. In this brief, we also propose an improved initial guess ψ'_{guess} for the computation of $\psi_{1\chi}$. ψ_{guess} mentioned in Fig. 1 in [2] is again used to arrive at a new guess ψ'_{guess}, i.e.,

$$\psi'_{\text{guess}} = V + \frac{1}{\beta}\ln\left(\frac{\left[\frac{2\pi}{\beta t_{\text{si}}}\right]^2 + \left[\frac{C_{\text{ox1}}}{\epsilon_{\text{si}}}(V_{gs1} - \psi_{\text{guess}})\right]^2}{B}\right). \tag{2}$$

This ensures a faster convergence of Halley's iterative loop used in computing $\psi_{1\chi}$ under all bias conditions.

Fig. 2 shows the effect of change in the upper bound to $\psi_{1\chi}$ over the performance of these algorithms. Here, the LZ4 algorithm is observed to be superior to all the other root-finding methods consistently. A slightly wider solution space due to a change in the upper bound seemed to degrade the performance of the LZ3, Brent, and Alefeld–Potra algorithms, whereas the performance of Dekker and LZ4 remained almost unaffected. There is an improvement of about 12%–15% in the LZ4 algorithm over Fig. 1, resulting from the simplification in the computation of the upper bound.

TABLE II
PERFORMANCE COMPARISON OF OLD AND NEW ALGORITHM AS SEEN IN A CIRCUIT SIMULATOR

Circuit	Tied-gate			Untied-gate			Tied/Untied Old	Tied/Untied New
	Old (s)	New (s)	% Improvement	Old (s)	New (s)	% Improvement		
51-stage ring oscillator	168.63	57.22	66	51.06	47.98	6	3.30	1.19
8-bit twisted ring counter	69.55	24.97	64	37.8	33.29	12	1.83	0.75
8-bit ripple adder	42.99	17.52	59	30.05	23.01	23	1.43	0.76

III. IMPLEMENTATION AND CIRCUIT SIMULATION

The proposed IVE solution technique is implemented in a professional circuit simulator, SmartSpice [9], using the Verilog-A interface. A 51-stage ring oscillator, a 8-bit ripple adder, and a 8-bit twisted ring counter (Johnson counter) were designed using the IDG MOSFET device with $t_{\rm si} = 30$ nm, $t_{\rm ox1} = 3$ nm, $t_{\rm ox2} = 2$ nm, and $\Delta\phi_{1(2)} = 0$. Two different circuit design approaches were adopted, i.e., circuits using tied-gate configuration, where the transistor always operates in the trigonometric mode, and circuits where the second gate is deactivated (grounded or connected to the source) so that the transistor operation is predominantly in the hyperbolic mode. The circuit simulation time with the proposed algorithm was compared against that for the existing method [2]. The simulation time recorded in Table II is the mean value obtained after three repeated simulation runs. All the simulations are run on a Intel Xeon E5472 eight-processor single-core 2400-MHz-speed 6144-KB cache with a 16-GB random access memory machine, using the 4.3.2.c version of SmartSpice. To record the timings in SmartSpice, we use the command ".options ACCT = 2" in the netlist file and check for "VLGP" in "Device Loads" section in the logfile. The entries in column "old" refer to the simulation time for the technique mentioned in [2], and those in "new" refer to our proposed method.

As shown in Table II, the simulation time for circuits using tied-gate devices is reduced by an average 60% with the proposed solution technique when compared with the old technique, which employed Ridders RBM. In the case of circuits with untied-gate device configurations, an average improvement of 15% in the simulation time is observed over the NR algorithm-dominated previous technique. Furthermore, it can be observed that, with the proposed technique, the ratio of simulation times for tied-gate configurations to untied-gate configurations approaches unity, hence reducing the disparity in the computational effort between the trigonometric and hyperbolic modes that previously existed. These results clearly demonstrate the superiority and the efficiency of the proposed solution technique over the existing hybrid solution technique when implemented in a circuit simulator.

IV. CONCLUSION

A single RBM has been proposed to solve the IVEs of the IDG MOSFET across all bias conditions. The proposed algorithm uses only the function values and completely eliminates the need for derivative computation. It converges much faster than the existing hybrid technique without compromising the root accuracy. A simpler upper bound for the root of the trigonometric IVE has been proposed, which further reduces the computation time by 12%–15%. The proposed IVE solution has been implemented in a professional circuit simulator, SmartSpice, using the Verilog-A interface. The simulation of circuit blocks such as the ring oscillator, the ripple adder, and the counter confirms the superior timing performance of the proposed technique over the existing technique.

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REFERENCES

[1] A. Sahoo, P. K. Thakur, and S. Mahapatra, "A computationally efficient generalized Poisson solution for independent double gate transistors," *IEEE Trans. Electron Devices*, vol. 57, no. 3, pp. 632–636, Mar. 2010.
[2] S. Jandhyala and S. Mahapatra, "An efficient robust algorithm for the surface potential calculation of independent DG MOSFET," *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1663–1671, Jun. 2011.
[3] C. J. F. Ridders, "Three-point iterations derived from exponential curve fitting," *IEEE Trans. Circuits Syst.*, vol. CAS-26, no. 8, pp. 669–670, Aug. 1979.
[4] R. P. Brent, "An algorithm with guaranteed convergence for finding a zero of a function," *Comput. J.*, vol. 14, no. 4, pp. 422–425, Mar. 1971.
[5] J. C. P. Bus and T. J. Dekker, "Two efficient algorithms with guaranteed convergence for finding a zero of a function," *ACM Trans. Math. Softw.*, vol. 1, no. 4, pp. 330–345, Dec. 1975.
[6] G. Alefeld, F. A. Potra, and Y. Shi, "Enclosing zeros of continuous functions," *ACM Trans. Math. Softw.*, vol. 21, no. 3, pp. 327–344, Sep. 1995.
[7] D. Le, "Three new rapidly converging algorithms for finding a zero of a function," *SIAM J. Sci. Stat. Comput.*, vol. 6, no. 1, pp. 193–208, Jan. 1985.
[8] D. Le, "An efficient derivative-free method for solving nonlinear equations," *ACM Trans. Math. Softw.*, vol. 11, no. 3, pp. 250–262, Sep. 1985.
[9] *Smartspice, Analog Circuit Simulator Version 4.3.2, Users' Manual*, Silvaco Int., Santa Clara, CA, 2010. [Online]. Available: www.silvaco.com

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