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Continuity equation based nonquasi-static charge model for independent double gate MOSFET

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Abstract Using the numerical device simulation we show that the relationship between the surface potentials along the channel in any double gate (DG) MOSFET remains invariant in QS (quasistatic) and NQS (nonquasi-static) condition for the same terminal voltages. This concept along with the recently proposed 'piecewise charge linearization' technique is then used to develop the intrinsic NQS charge model for a Independent DG (IDG) MOSFET by solving the governing continuity equation. It is also demonstrated that unlike the usual MOSFET transcapacitances, the inter-gate transcapacitance of a IDG-MOSFET initially increases with the frequency and then saturates, which might find novel analog circuit application. The proposed NQS model shows good agreement with numerical device simulations and appears to be useful for efficient circuit simulation.

Keywords Compact modeling · Nonquasi static (NQS) effect · Double gate (DG) MOSFET

1 Introduction

Independent double gate MOSFET (IDG-MOSFET) are being attractive for several novel circuit applications [1–3] due to its ability to modulate threshold voltage and transconductance dynamically. The BSIM-IMG model [4], which is currently under evaluation for CMC standardization, is applicable for a particular form of IDG-MOSFET [5], where the back gate oxide thickness is much higher than the front gate oxide thickness so that the front gate acts as high frequency gate while the back gate is used for controlling the threshold voltage. Therefore this model is not valid for a generic IDG MOSFET, where both gates independently can act as high-frequency gates. Recently two independent research groups have reported quasistatic (QS) compact charge models [6–8] for such generic IDG transistors. While the first group [6] proposes to extend the 'symmetric charge linearization' technique, which was used extensively in bulk MOSFET modeling, for the charge modeling of IDG MOSFET, the other group [7] argues that such conventional linearization technique cannot be applied to IDG MOSFET due to the possible non-linear relationship between the surface potentials. To overcome this problem, 'piecewise linearization technique' is proposed in which the channel is segmented in few sections using 'secondary input voltage equation (S-IVE)' so that the conventional linearization technique could be applied to each section.

For successful utilization of these devices in RF circuit design, one needs to include nonquasi-static (NQS) effects [9] in the charge model. Two methodologies, continuity equation (CE) [10] based and relaxation time approximation (RTA) [11–13], are being used to model NQS effect in professional compact models for MOS transistors. The CE based approach is physically based and thus applicable to very high frequency range. However it is computationally expensive because of its mathematical complexity. On the other hand the RTA based approach is semi-empirical in nature, and thus not applicable for very high frequency range, however it is computationally efficient due to its simple mathematical formulation.

In this work we use the surface potential relation along with the 'piecewise charge linearization' technique to develop the NQS charge model for the intrinsic part of a IDG

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MOSFET by solving the governing continuity equation. We demonstrate that unlike the usual MOSFET transcapacitances, the inter-gate transcapacitance of a IDG-MOSFET initially increases with the frequency and then saturates, which might be attractive for novel analog circuit application. The proposed NQS model shows good agreement with TCAD [14] simulations and appears to be useful for efficient circuit simulation. The CE based NQS models for common double-gate MOSFET are reported elsewhere [15, 16].

2 Model development

The conventions used in this paper are: $t_{ox1(2)}$ is the oxide thickness of first (second) gate, t_{si} is the thickness of the silicon body, $C_{ox1(2)}$ is the oxide capacitance per unit area of first(second)-gate defined as $\varepsilon_{ox}/t_{ox1(2)}$, ε_{si}, ε_{ox} are the permittivities of Si and SiO_2 respectively, q is the elementary charge, $\beta = q/kT$ is the inverse thermal voltage where k and T represent Boltzmann constant and temperature in Kelvin respectively, n_i is the intrinsic carrier density, $B = 2qn_i/\beta\varepsilon_{si}$, L is the channel length, W is the channel width, $\psi_{1(2)}$ are the Si/SiO_2 surface potentials at first(second) gate, V is the electron quasi-Fermi potential (channel potential) and μ is the effective mobility. The effective gate voltage is defined as $V_{gs1(2)} = V_{gs1(2)_{applied}} - \delta\phi_{1(2)}$, where $V_{gs1(2)_{applied}}$ is the voltage applied at gate terminals and $\delta\phi_{1(2)}$ is the work function difference of the gate material. The inversion charge density at any point along the channel is denoted by Q_i, which is sum of two components Q_{i1} and Q_{i2} expressed as $Q_{i1(2)} = C_{ox1(2)}(V_{gs1(2)} - \psi_{1(2)})$. In following discussions, any variable with subscript 's' refers to its values at source end and 'd' refers to its value at drain end.

The governing continuity equation for a IDG MOSFET can be expressed as

$$\frac{\partial I}{\partial y} = -W\frac{\partial Q_i}{\partial t} \Rightarrow \frac{\partial}{\partial y}\left(\mu W Q_i \frac{dV}{dy}\right) = -W\frac{\partial Q_i}{\partial t} \tag{1}$$

where I is the drain current and V is the channel potential at any point y along the channel ($y = 0$ and L represents source and drain end respectively). Now from the expression of the coupling factor G ((4) in [17]) we arrive at

$$V = V_{gs1} - \frac{Q_{i1}}{C_{ox1}} - \frac{1}{\beta}\ln\left(\frac{1}{B}\left(nQ_{i1}^2 - G\right)\right) \tag{2}$$

where $n = 1/\varepsilon_{si}^2$. Further applying linearisation $G \simeq s_1 Q_{i1} + k_1$ [17], and differentiating (2) w.r.t. Q_{i1} we obtain

$$\frac{dV}{dQ_{i1}} = -\frac{1}{C_{ox1}} - \frac{1}{\beta}\frac{(2nQ_{i1} + s_1)}{(nQ_{i1}^2 + s_1 Q_{i1} + k_1)} \tag{3}$$

with $s_1 = (G_s - G_d)/(Q_{i1d} - Q_{i1s})$ and $k_1 = -(G_s Q_{i1d} - G_d Q_{i1s})/(Q_{i1d} - Q_{i1s})$.

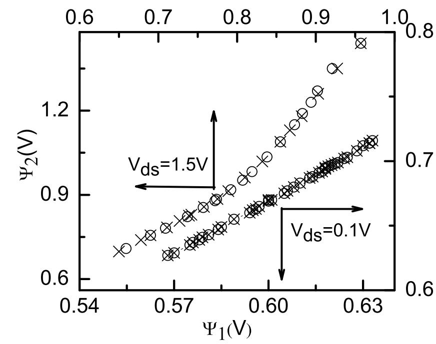

Fig. 1 Relationship between ψ_1 and ψ_2 in both linear and saturation region at $V_{gs1} = 1.5$ V, $V_{gs2} = 0.7$ V. *Circle* represents NQS condition and *Cross* represents QS condition. QS results are obtained by DC simulation in TCAD while NQS results are obtained through transient simulation by ramping the V_{gs1} from 1 V to 1.5 V in 50 ps

Unlike a common double gate (CDG) MOSFET, the surface potentials along the channel in a IDG MOSFET might not hold a linear relationship for a given bias conditions [7]. Therefore the same linearization technique (i.e. (4) in [16]) cannot be used here. However by TCAD simulation (Fig. 1), we observe that the relationship between the surface potential for a given terminal voltages remains same irrespective of QS or NQS condition. Therefore if we develop an analytic relation between ψ_1 and ψ_2 under QS condition it should remains valid under NQS condition for the same set of terminal voltages. In order to develop an analytic relationship between Q_i and Q_{i1} (it is imperative that similar to ψ_1 and ψ_2, the relationship between Q_i and Q_{i1} remains invariant under NQS and QS condition) we use the *four* segment piecewise linearization technique [7]. By solving the S-IVE at the three break-points (Table I in [7]) we can obtain Q_i and Q_{i1} values at three different locations inside the channel for a given bias condition. We can then formulate the following fourth order relationship

$$Q_{i1} = c_1 Q_i^4 + c_2 Q_i^3 + c_3 Q_i^2 + c_4 Q_i + c_5 \tag{4}$$

where the coefficients (c_1 to c_5) are obtained by solving the following set of five linear equations at source and drain ends and at the three break-points.

$$Q_{i1s} = c_1 Q_{is}^4 + c_2 Q_{is}^3 + c_3 Q_{is}^2 + c_4 Q_{is} + c_5 \tag{5}$$

$$Q_{i1_1} = c_1 Q_{i_1}^4 + c_2 Q_{i_1}^3 + c_3 Q_{i_1}^2 + c_4 Q_{i_1} + c_5 \tag{6}$$

$$Q_{i1_2} = c_1 Q_{i_2}^4 + c_2 Q_{i_2}^3 + c_3 Q_{i_2}^2 + c_4 Q_{i_2} + c_5 \tag{7}$$

$$Q_{i1_3} = c_1 Q_{i_3}^4 + c_2 Q_{i_3}^3 + c_3 Q_{i_3}^2 + c_4 Q_{i_3} + c_5 \tag{8}$$

$$Q_{i1d} = c_1 Q_{id}^4 + c_2 Q_{id}^3 + c_3 Q_{id}^2 + c_4 Q_{id} + c_5 \tag{9}$$

where Q_{i1_1}, Q_{i1_2} and Q_{i1_3} represents the inversion charges across the front channel at three break points and Q_{i_1}, Q_{i_2} and Q_{i_3} represents the total inversion charges at three break

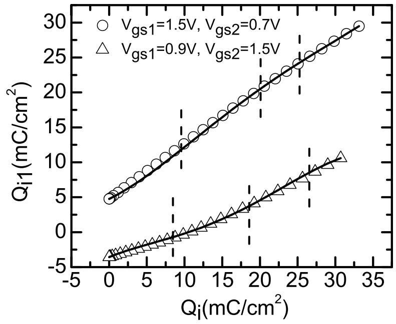

Fig. 2 Relationship between Q_i and Q_{i1} for two different bias conditions. *Symbol* represents the exact relationship and *line* represents approximated fourth order relationship. *Vertical dash lines* represent the break points

points. Figure 2 shows that such fourth order polynomial approximation for Q_{i1} in terms of Q_i is quite accurate.

Using (9) and (3) in (1) and introducing normalized variables: $y' = y/L$, $t' = t/\frac{L^2}{\mu}$, we obtain the modified form (1) as

$$\frac{\partial Q_i}{\partial t'} = \frac{\partial^2 Q_i}{\partial y'^2} f(Q_i) + u(Q_i)\left(\frac{\partial Q_i}{\partial y'}\right)^2 \tag{10}$$

where

$$f(Q_i) = \xi.\vartheta Q_i \tag{11}$$

$$u(Q_i) = \Upsilon + \frac{Q_i \vartheta \varpi}{\beta(nQ_{i1}^2 + s_1 Q_{i1} + k_1)^2} \tag{12}$$

with

$$\xi = 1/C_{ox1} + (2nQ_{i1} + s_1)/\big(nQ_{i1}^2 + s_1 Q_{i1} + k_1\big)\beta \tag{13}$$

$$\vartheta = 4c_1 Q_i^3 + 3c_2 Q_i^2 + 2c_3 Q_i + c_4 \tag{14}$$

$$\varpi = \big(2n\vartheta\big(nQ_{i1}^2 + s_1 Q_{i1} + k_1\big)\big) - \big(\vartheta(2nQ_{i1} + s_1)^2\big) \tag{15}$$

and

$$\Upsilon = \xi\big(16c_1 Q_i^3 + 9c_2 Q_i^2 + 4c_3 Q_i + c_4\big) \tag{16}$$

To obtain the Q_i distribution over y at time t, we need to solve (10) with the boundary condition $Q_i(y=0,t) = Q_{is}$ and $Q_i(y=L,t) = Q_{id}$ and the initial condition $Q_i(y,0)$, which could be obtained by evaluating the y versus L relationship for each segment [7] and then inverting it to get Q_i for any y. Similar to the CDG MOSFET model [16] we assume no NQS effect at source and drain end so that Q_{is} and Q_{id} can be calculated by solving the primary input voltage equations (P-IVE) [7, 18] for the bias conditions at time t. Once we obtain $Q_i(y,t)$, the terminal charges could be computed by solving the terminal charge integrals ((6)–(9) in [7]). In order to solve (10) we convert it in a system of ordinary differential equations (ODEs) by spline collocation method [19], which could be solved inside a circuit simulator by sub-circuit approach. In this work we solve them in MATLAB [20] by four-point spline collocation method. In a four point spline collocation method, if the inversion charges are defined as $q_0 = Q_i(y'=0) = Q_{is}$, $q_1 = Q_i(y'=1/5)$, $q_2 = Q_i(y'=2/5)$, $q_3 = Q_i(y'=3/5)$, $q_4 = Q_i(y'=4/5)$, and $q_5 = q(y'=1) = Q_{id}$, (10) could be converted into following four coupled ODEs [10, 15]

$$\frac{dq_j}{dt'} = a_j f(q_j) + u(q_j)(b_j)^2 \tag{17}$$

where j varies from 1 to 4 and

$$a_1 = \frac{1350q_2 - 1905q_1 - 360q_3 + 90q_4 - 15q_5 + 840q_0}{209/10} \tag{18}$$

$$a_2 = \frac{1350q_1 - 2265q_2 + 1440q_3 - 360q_4 + 60q_5 - 225q_0}{209/10} \tag{19}$$

$$a_3 = \frac{1440q_2 - 360q_1 - 2265q_3 + 1350q_4 - 225q_5 + 60q_0}{209/10} \tag{20}$$

$$a_4 = \frac{90q_1 - 360q_2 + 1350q_3 - 1905q_4 + 840q_5 - 15q_0}{209/10} \tag{21}$$

$$b_1 = \frac{900q_2 - 225q_1 - 240q_3 + 60q_4 - 10q_5 - 485q_0}{209} \tag{22}$$

$$b_2 = \frac{840q_3 - 15q_2 - 780q_1 - 210q_4 + 35q_5 + 130q_0}{209} \tag{23}$$

$$b_3 = \frac{210q_1 - 840q_2 + 15q_3 + 780q_4 - 130q_5 - 35q_0}{209} \tag{24}$$

$$b_4 = \frac{240q_2 - 900q_3 - 60q_1 + 225q_4 + 485q_5 + 10q_0}{209} \tag{25}$$

The charge distribution across the channel length $Q_i(y,t)$ in four point spline collocation method is of the form:

$$Q_i(y',t) = e_1 y'^3 + f_1 y'^2 + g_1 y' + h_1 \quad \big(0 \le y' \le 1/4\big) \tag{26}$$

$$Q_i(y',t) = e_2 y'^3 + f_2 y'^2 + g_2 y' + h_2 \quad \big(1/4 \le y' \le 2/4\big) \tag{27}$$

$$Q_i(y',t) = e_3 y'^3 + f_3 y'^2 + g_3 y' + h_3 \quad \big(2/4 \le y' \le 3/4\big) \tag{28}$$

$$Q_i(y',t) = e_4 y'^3 + f_4 y'^2 + g_4 y' + h_4 \quad \big(3/4 \le y' \le 4/4\big) \tag{29}$$

where the coefficients e_1, e_2, e_3, e_4, f_1, f_2, f_3, f_4, g_1, g_2, g_3, g_4, h_1, h_2, h_3 and h_4 is obtained by solving the four coupled ODEs, using which we solve the terminal charge integrals ((6)–(9) in [7]) to obtain the respective terminal charges.

3 Results and Discussions

We have validated our model against the 2-D TCAD simulation results [14] for devices having gate oxide thickness asymmetry: $t_{ox1} = 1$ nm, $t_{ox2} = 1.5$ nm, $t_{si} = 10$ nm, $L = 1$ µm, $W = 1$ µm. The channel is kept undoped and source-drain doping is taken as 10^{20} cm^{-3}. We use constant mobility of 300 $\text{cm}^2/\text{V s}$ both in TCAD simulation and proposed model. The cut-off frequency (f_t) with respect to the first gate is calculated as $f_t = \frac{g_{m1}}{2\pi C_{g1g1}}$, where g_{m1} is the front gate transconductance and C_{g1g1} is front gate-self capacitance. It is observed that saturation f_t (i.e., $V_{gs} = V_{ds} = 1$ V) changes from 1.87 GHz to 2.97 GHz as we change the second gate bias from 0.1 V to 1 V and the linear f_t (i.e., $V_{gs} = 1$ V, $V_{ds} = 0.1$ V) changes from 0.475 GHz to 0.478 GHz for the same.

Figure 3 shows the transient behaviour of terminal currents while the V_{gs1} changes from 0.5 to 1 V in 100 ps while V_{gs2} is kept constant at 0.5 V. In order to ensure that the transistor works in non-quasistatic condition the rise time of the carriers should be smaller than the transit time of the carriers. Therefore, here the rise time is chosen to be 100 ps which is less than the transit time ($1/f_t$), 383 ps of the carriers. We see that the currents predicted by the proposed NQS model matches very well with TCAD results as opposed to the QS model.

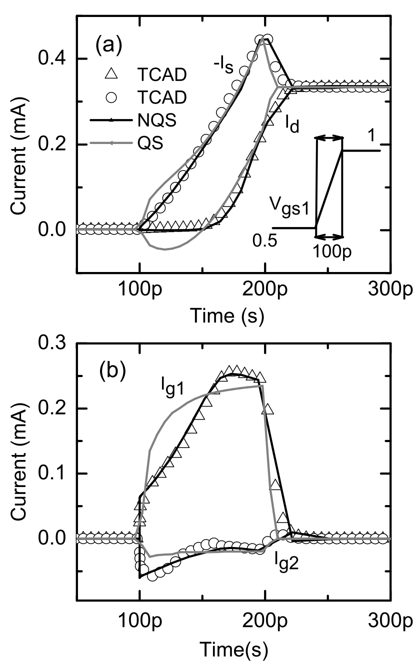

Fig. 3 (**a**) Drain (I_d) and source (I_s); (**b**) gate terminal currents predicted by proposed model and the TCAD simulation. A ramp voltage from 0.5 to 1 V is applied to front gate with a rise time of 100 ps, V_{gs2} is kept at 0.5 V and V_{ds} is kept at 1 V

Accurate calculation of the small signal Y parameters of a MOS transistors is very important for analog/RF circuit design. The Y_{eh} between any two terminals e and h for a IDG-MOSFET is represented as $Y_{eh} = \frac{\partial I_e}{\partial V_h}$ where I and V are the currents and voltages at those terminals while keeping other terminal voltages to be constant. Overall, there are 16 Y_{eh} parameters; among which 9 are independent and shown in Fig. 4. Any of the Y_{eh} can also be represented as $Y_{eh} = G_{eh} + j\omega C_{eh}$ where G_{eh} represents transconductance and C_{eh} represents trans-capacitance. The variation for the real and imaginary components of different Y parameters as a function of frequency is demonstrated in Fig. 4 under both saturation and linear bias conditions. To keep the brevity, we only show the Y parameters with respect to the front gate as the Y parameters with respect to the second gate follow the same trends. We see that with a 4-point collocation technique the proposed model predicts the Y parameters quite accurately at least for a frequency range of $8 f_t$ for saturation bias condition and $20 f_t$ for linear bias condition. Only for the saturation Y_{g1d}, Y_{g2d} and Y_{dd} characteristics,shown in Fig. 4(g)–(i), we use basic channel length modulation (CLM) model by introducing effective channel length as $L_{eff} = L \times (1 - \lambda V_{ds})$ where λ is taken to be 0.02 (as explained in [16]). It is worth noting that Y_{g1d}, Y_{g2d} and Y_{dd} in saturation is 100 times lower than its linear value and hence is not very significant for circuit design purpose. Figure 5 shows the variation in first gate Y-parameter, Y_{dg1} with variation in back gate bias V_{gs2}. It is observed that with change in back gate bias there is not much change in frequency response and also the proposed model shows good agreement with TCAD simulation results for all bias conditions.

One of the interesting NQS features of IDG MOSFET is the frequency response of its inter-gate transcapacitance as shown in Fig. 6. It is observed that unlike other transcapacitances, C_{g2g1} initially increases with frequency and then saturates to a particular value and the proposed model accurately predicts the characteristics. Such anomalous behaviour can be explained in following way. If we denote the first gate and second gate terminal charges by Q_{G1} and Q_{G2} respectively and the total inversion charge in the channel by Q_I, then to conserve the total charge $Q_{G1} + Q_{G2} + Q_I = 0$. Now for a change of first gate charge ΔQ_{G1}, the change in the second gate charge will be $\Delta Q_{G2} = -\Delta Q_{G1} - \Delta Q_I$. For a same ΔQ_{G1}, if we calculate ΔQ_{G2} at different frequency, we observe that due to finite transit time of the carriers in the channel, ΔQ_I decreases with increasing frequency and then approaches to zero. As a result, ΔQ_{G2} first increases with frequency and then becomes equal to ΔQ_{G1}. Such unique inter-gate transcapacitance behaviour of IDG MOSFET might find novel analog/RF circuit application.

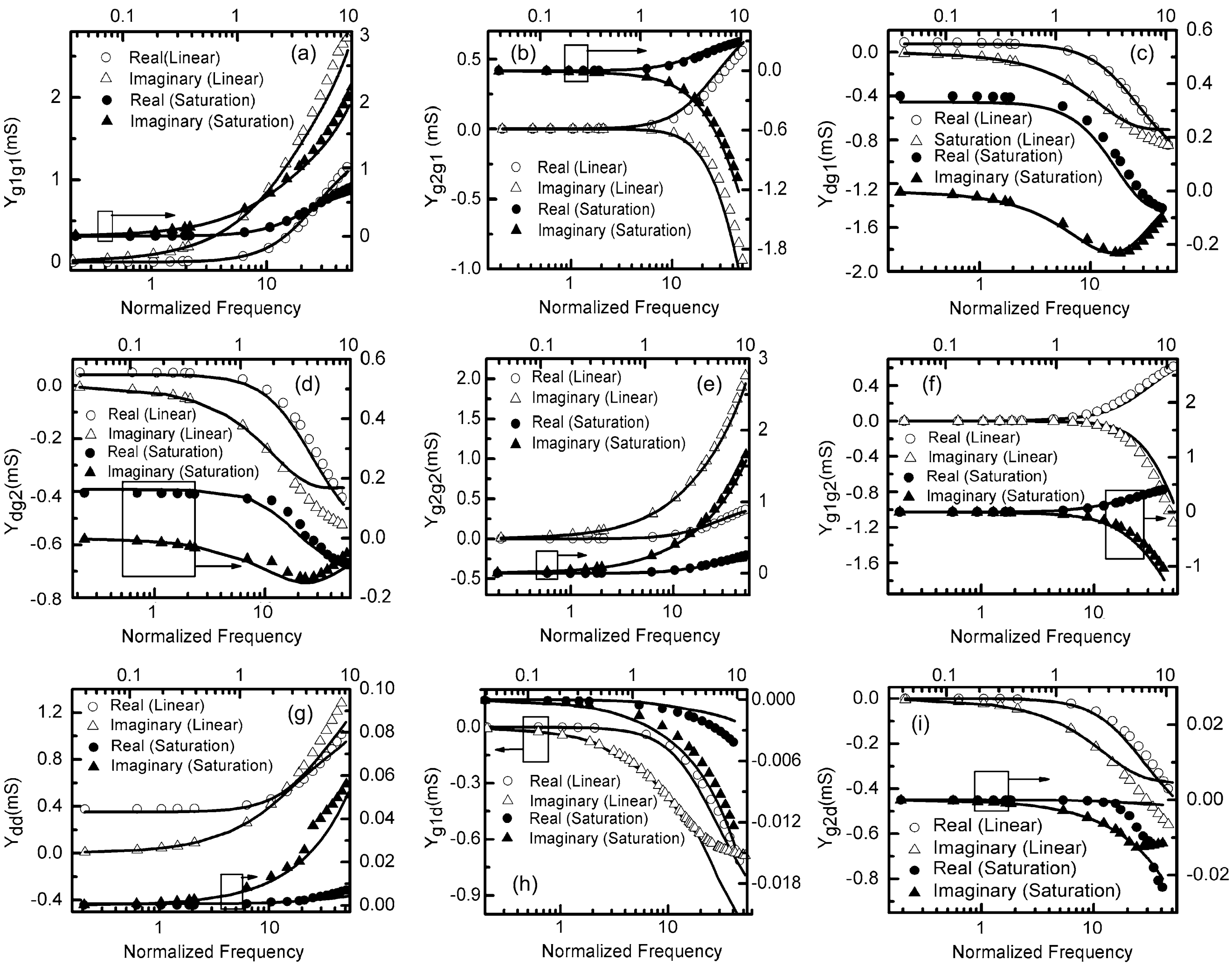

Fig. 4 Small signal characteristics: **(a)** Y_{g1g1}, **(b)** Y_{g2g1}, **(c)** Y_{dg1}, **(d)** Y_{dg2}, **(e)** Y_{g2g2}, **(f)** Y_{g1g2}, **(g)** Y_{dd}, **(h)** Y_{g1d}, and **(i)** Y_{g2d}, as predicted by the TCAD (*symbol*) and the proposed model (*line*). In all plots V_{gs1} and V_{gs2} are kept at 1 V and 0.7 V respectively. Y at $V_{ds} = 1$ V is plotted against top x-axis, which is normalized to 2.6 GHz (saturation f_t) and Y at $V_{ds} = 0.1$ V is plotted against bottom x-axis, which is normalized to 0.478 GHZ (linear f_t)

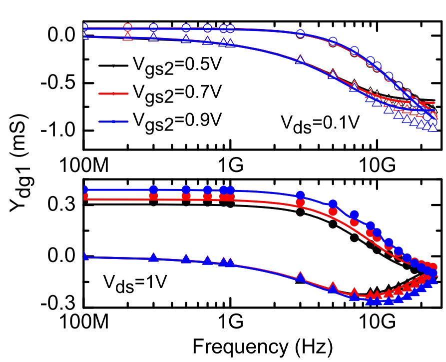

Fig. 5 Relationship between Y_{dg1} in both linear and saturation region. *Line* represents the model and *symbol* represents TCAD data. In all the plots V_{gs1} is kept at 1 V. Saturation f_t values are 2.36 GHz, 2.6 GHz, 2.85 GHz for $V_{gs2} = 0.5$ V, 0.7 V, 0.9 V respectively, while the linear f_t remains almost at 0.478 GHz for all V_{gs2}

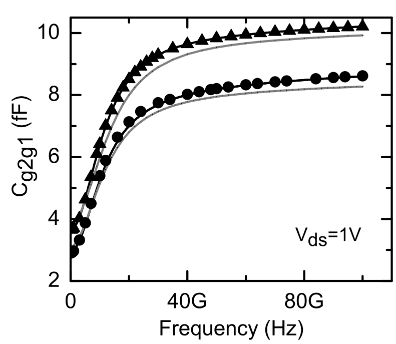

Fig. 6 Frequency response of C_{g2g1} at $V_{gs1} = 1$ V. *Circle* represents $V_{gs2} = 0.7$ V and *triangle* represents $V_{gs2} = 0.9$ V. *Black line* represents exact solution of (10), while the *gray line* represents 4-point collocation method based solution

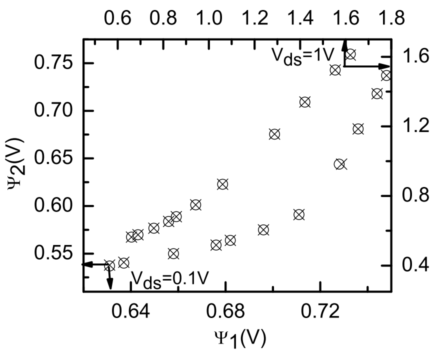

Fig. 7 Relationship between ψ_1 and ψ_2 in both linear and saturation region at $V_{gs1} = 1.5$ V, $V_{gs2} = 0.7$ V with incorporation of velocity saturation. *Circle* represents NQS condition and *Cross* represents QS condition. QS results are obtained by DC simulation in TCAD while NQS results are obtained through transient simulation by ramping the V_{gs1} from 1 V to 1.5 V in 50 ps

All the results presented above are for long channel IDG MOSFET. In inclusion of small-geometry effects require further research and out-of-scope of the present manuscript. However from TCAD simulation it is observed (Fig. 7) that even in short channel MOSFET ($t_{ox1} = 1$ nm, $t_{ox2} = 2$ nm, $t_{si} = 10$ nm, $L = 30$ nm, $W = 1$ μm) with incorporation of velocity saturation effect the surface potentials across the two channel holds same relationship in both QS and NQS for a particular bias condition. Quantum mechanical effect (QME) has not been included here because transient simulation with QME model is not possible in TCAD simulation [14]. Therefore, in order to model NQS effects in short channel IDG MOSFETs we can use the same approximation as adopted for long channel IDG MOSFETs.

Finally, it is worth noting that once the QS charge are calculated, the complexity of the proposed IDG MOSFET NQS model is the same order as of the CDG MOSFET NQS model [16]. However, because of the piecewise charge linearization technique the IDG MOSFET QS model is computationally expensive than that of CDG MOSFET.

4 Conclusion

Based on the relationship between the surface potentials and piecewise linearization technique, we propose a continuity equation based new NQS charge model for independent double gate MOSFETs. Proposed models have been verified against TCAD simulation and appears to be useful for RF circuit simulation.

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