Real-Time Image Segmentation Using Neuromorphic Pixel Array

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***Abstract*—Image segmentation is a critical step in achieving computer vision. For fast and near real time image segmentation it is important to use dedicated hardware as it works much faster as compared to software based solutions. This paper presents a CMOS based real time image segmentation analog circuit using semi-supervised learning scheme. The proposed circuit ensures minimal operating power required when compared to its digital hardware implementation due to sub-threshold region operation of MOSFET and much lesser number of transistors being used. The circuit operation is based upon an anisotropic current spreading in non linear circuits. An analog pixel array is created which takes in weights and initial seed as input and segments the image based on them. Weights are generated from an image based on the feature similarity and are then fed to the pixel array. These weights dictate the anisotropic diffusion of current in the analog array and thus required segmentation is achieved. The proposed analog circuit based segmentation scheme is highly power efficient as compared to digital hardware implementation. Thus this scheme can be used in a power constrained environment as in case of Internet of Things (IoTs) network with independent battery-less nodes. Our approach will also be suitable for applications that require high-performance computing to run in real time, such as biomedical image segmentation for image-guided surgery.**

***Index Terms*—Real-time image segmentation; Random walker algorithm; Pixel array; Laplace equation; Graph theory**

I. INTRODUCTION

A key component of computer vision is effective and fast image segmentation and many algorithms have been proposed to achieve this. Image segmentation divides an image into set of different pixel regions. These regions have pixels that are grouped together based on their similarity in a particular image attribute (feature). These classifying features can be color, gray scale or texture. Several image segmentation techniques are popular [1], [2] and all these techniques are broadly classified into three categories namely manual, semi automatic and fully automatic [2], [3]. In this work, the semi automatic scheme is used which requires minimal initial user interaction and is very effective. This work involves analog implementation of segmentation in which the initial seed is represented by a voltage which in turn generates an appropriate current that diffuses into the circuit based on the weights. Weights for different pixels in the circuit is decided by some pre-decided image feature.

The overall scheme used for segmentation is based on the random walker algorithm (RW) [4]. The RW algorithm models the image as a pixel array where each pixel is connected to its neighboring pixels by weights. Segmentation is achieved by the RW algorithm by solving a discrete Dirchlet problem [5], [6]. However, solving this is computationally very expensive which limits its use in case of real time applications. To use this algorithm we need to find a way to implement this in hardware such that it runs faster and thus becomes usable in real time scenario.

Several hardware implementations are being reported in the digital domain using FPGAs [7]- [9] . However, as the number of transistors used are much more than in a typical analog implementation solution (presented in this work) the power consumption is higher. Higher power consumption limits the use of digital hardware in end nodes of systems as in a IoT network where power consumption may be critical. The proposed analog array implementation may find several applications in the power constrained scenarios such as in the IoT, as the circuit operates in the sub-threshold region of transistor. A typical use case may be in image guided surgery [10], [11] that uses image segmentation.

Neuromorphic circuits can be used to develop systems that are suited for low power and real-time applications [12]- [16]. As the circuit operate in the sub-threshold region of a transistor, the power consumed is order of magnitudes lower than in other implementations used for achieving the same target application.

This work presents an implementation of image segmentation algorithm employing neuromorphic circuit. In this implementation, images are segmented by solving a discrete partial differential equation using an iterative method. Typically, a scene is partitioned into different objects based on common properties such as depth, motion, or image intensity. This work uses image intensity as the basis for segmentation, but other properties such as texture or color can also be used for segmentation. As the RW algorithm is based on semi supervised learning, an initial seed for object segmentation is required.

This work initially describes the RW algorithm used in developing a pixel array for real time image processing. Further the analog circuit used for segmentation is explained and the overall system topology is mentioned. Using this circuit, segmentation is successfully obtained for various images. Analysis of the power usage and area of the chip required is done based on the layout and other circuit parameters.

II. Algorithmic Framework

A. Random Walker Algorithm

The RW algorithm is a graph-based semi-automatic image segmentation scheme, where a user or pre-processing algorithm assigns the labels (either foreground or background) for a few image pixels. These pixels serve as initial seed points for performing the segmentation task as in the case of semi supervised learning. The algorithm works on a weighted graph framework [17], where each node represents a pixel. The nodes are connected to each other by graph edges and each connection is assigned an appropriate weight. The weights are treated as a penalty (or cost function) for traversing from one pixel to another along an edge. Among the connecting edges in the graph, weights to different edges are assigned such that the desirable regions (object parts to be segmented) in the image have higher weight connections and vice versa. An image can be represented as a graph G =(V, E), which consists of vertices V and edges E. For two nodes v_i and v_j, the corresponding interconnection edge and weight are e_{ij} and w_{ij} respectively. Weights are considered as unidirectional and positive. Weights are computed by processing the image based on features such as pixel intensity, texture and color. Here, we consider image intensity as the processing feature and use the Gaussian weighting function, expressed as:

$$w_{ij} = \exp(-\beta(g_i - g_j)^2) \tag{1}$$

where,g_i is the image intensity at pixel i and β is the free parameter. For a colour image, g_i will represent a vector that handles different colour channels. Equation (1) can be modified to apply other image features such as texture or color information. In semi-automatic segmentation algorithm, there are a set of user-defined nodes (pixels) denoted as V_m which are few in number, and a set of unmarked pixels V_u. In case of binary-labelled segmentation,each predefined node V_m is labelled from C = 0,1, where 0 and 1 denote the background and foreground, respectively. Using V_m, all V_u have to be classified in set C. Segmentation is complete when all the unlabelled nodes V_u are assigned labels. This problem can be formulated as a diffusion process defined using the equation below:

$$\frac{\partial I}{\partial t} = \frac{\partial^2 I}{\partial x^2} + \frac{\partial^2 I}{\partial y^2} \tag{2}$$

where, I is an image in 2D space and $I_{x,y}$ denotes pixel intensity at position (x,y). Considering all edges to have same weights (isotropic diffusion) discrete formulation of Equation (2) can be written as:

$$I_{x,y}^{t+1} = I_{x,y}^{t} + \frac{1}{4}(I_{x-1,y} + I_{x+1,y} + I_{x,y-1} + I_{x,y+1} - 4I_{x,y}) \tag{3}$$

For edges with different weights the equation can be modified as:

$$\begin{aligned} I_{x,y}^{t+1} = I_{x,y}^{t} + \frac{1}{d_{x,y}}(&w_{x-1,y}I_{x-1,y} + w_{x+1,y}I_{x+1,y} \\ &+ w_{x,y-1}I_{x,y-1} + w_{x,y+1}I_{x,y+1} - d_{x,y}I_{x,y}) \end{aligned} \tag{4}$$

Equation (3) and (4) can be used to model the image with same weights throughout or different weights respectively. So the intensity at a particular pixel is related to intensity of the pixels in vicinity. Overall algorithm can be summarized as follows:

• For a given image, using the desired feature, weights for all

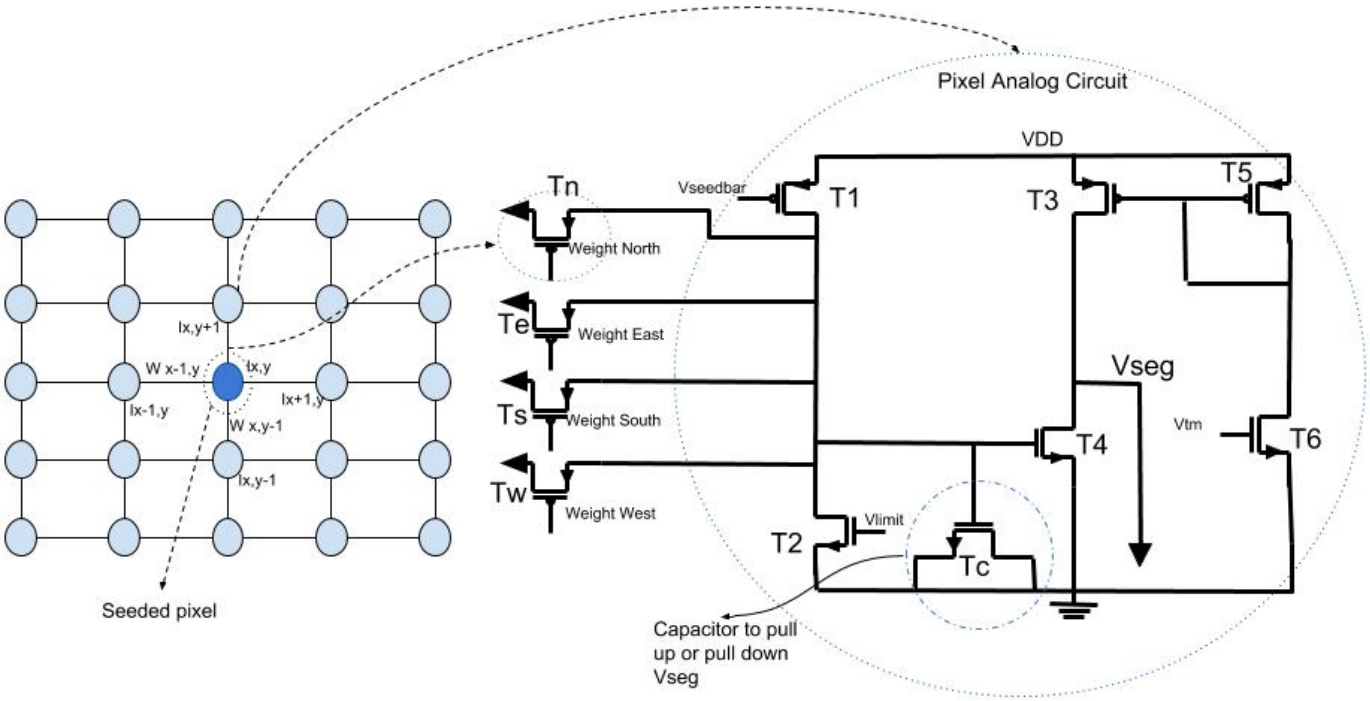


Fig. 1: 5x5 Analog Array with elaborated pixel analog circuit

the edges are calculated using neighborhood vicinity. Starting at the seeded nodes, weights for neighbouring pixels are generated and this is built upon throughout the image.

• After deciding upon the weights, these weights are passed on the analog pixel array where the current diffusion from a seeded pixel is decided by the connecting weights.

• Finally by current diffusion voltages are generated at each pixel, which depict whether that particular pixel is a part of foreground or background.

III. Circuit Implementation

A. Analog CMOS based implementation

The diffusion equation for a weighted graph proposed in the previous section can be represented as a spread of electrical charge in a RC circuit [18]. But this RC circuit can be further simplified if we use MOS in place of resistors and capacitors to reduce the chip area significantly. As known, the conductivity of the MOS can be controlled by the gate voltage V_{gs} applied to it. The proposed circuit [18]- [19] for a single pixel is shown in Figure 1. The circuit has a seed PMOS (transistor T1) and the seed is enable (connected to ground) for V_m pixels and disable (connected to V_{dd}) for V_u pixels. The current flowing in the circuit is further propagated based on the connecting weights in the directions north, south, east and west. MOS connected to V_{limit} is the current controlling MOS. V_{gs} to this MOS can be fixed to an appropriate value so as to allow a desirable amount of the current to diffuse further.

The preferred region of operation for this circuit is the sub-threshold region, which is used for low power consumption and because the operating current is low, handling of overall circuit is much easier. The current voltage relationship in this region is given by the following:

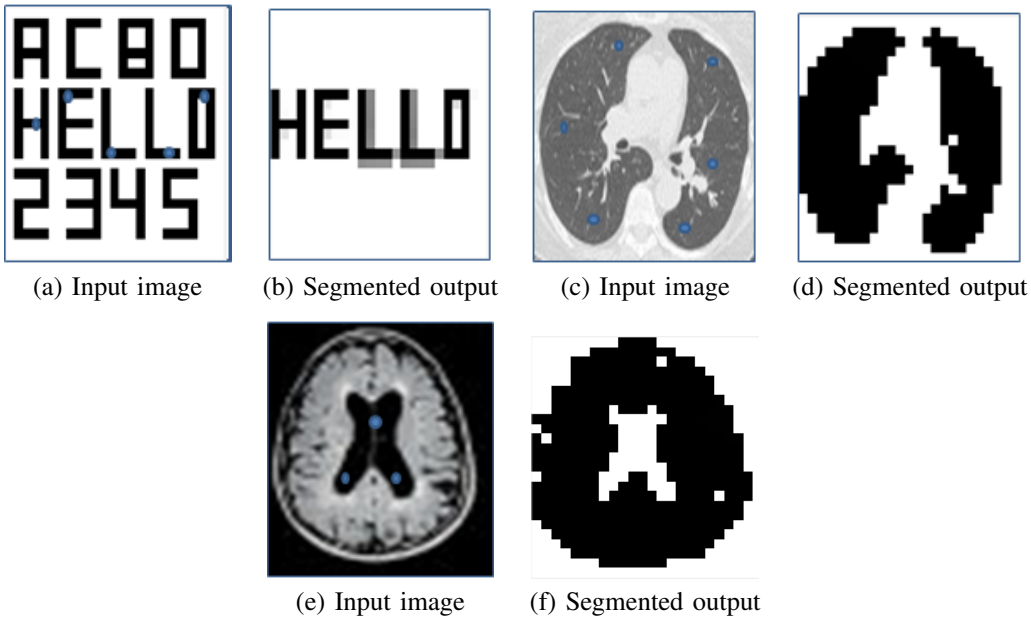
$$I_{ds} = I_{d0} \exp(V_{gs} - V_{ds})/\eta V_T \tag{5}$$

where, I_{d0} is the residual saturation drain current, η is the slope factor (generally between 1 and 1.5), and V_T is the thermal voltage. Weights for connecting edges can be varied by changing V_{gs} of the MOS transistors connected [19].

B. Single Pixel Circuit topology

The circuit (Figure 1) was designed using 65 nm technology with 1.2V supply voltage. In this circuit topology, a capacitor is required to pull up or pull down V_{seg} voltage. V_{seg} voltage is indicative of whether a pixel belongs to foreground or background. As the capacitor takes a large area in chip fabrication, it has been replaced by a MOS which has its drain, body and source tied to ground potential.Voltage V_{tm} is used to keep transistor T6 in saturation.

Transistor T2 is the current limiting device. In the unseeded node, current higher than that in T2 will charge the capacitor MOS so that the node belongs to the image foreground, as labelled by the seeded node. On the other hand, if the current in the unseeded node is less than current in T2 then V_{seg} will be pulled high and the pixel will be a part of the image background. This arrangement of analog pixels allows voltage propagation in the more conducting direction, set by weights (V_{gs} to the connecting transistors Tn, Te, Ts and Tw) and conducts segmentation as per the seeded nodes. Transistors T3 and T5 form a current mirror, which forces current in T4 and thus sets V_{seg} according to the voltage across the capacitor.



(a) Input image (b) Segmented output (c) Input image (d) Segmented output

(e) Input image (f) Segmented output

Fig. 2: Segmentation results obtained from a 25x25 pixel array.

IV. Results and Discussions

A. Segmentation results

The pixel circuit (Figure 1) was used to create a pixel array and the corresponding weight connections (V_{gs} of the PMOS connecting two pixels) are generated from the image. The weights of the image are calculated using Equation 1, but in future implementation, we will be using a circuit of finding the similarity between pixels along with the Pixel Circuit (Fig 1). One of such circuit could be the Bump circuit [20]. In this work, binary weights are generated based on predefined threshold corresponding to the foreground and background. After feeding the weights to the pixel array, the corresponding segmentation voltages from each pixel are generated. This voltage classifies the pixel as foreground or background. The voltage V_{seg} is low for pixels belonging to foreground and high for pixels belonging to background. The time required for the diffusion is corresponding to equivalent RC time constant obtained from the connecting transistors [19].

Figure 2 shows the segmentation results for different images fed to the analog array. Blue markers in the figure show the location of the seeds, which is user defined. Figure 2 (b) shows the segmented word "HELLO" of Figure 2 (a). Here a single seed point is given for each alphabet as a part of semi-supervised learning. Currently, we have used the binary weights, but can be extended to quantized levels for providing weights to further improve processing of gray scale and coloured images. Here multiple seeds were provided in different regions of the object of interest. Figure 2 (c, d, e, f) shows segmentation on thoracic cavity and MRI scans of brain respectively. For clinical purposes this type of segmentation can be very useful for better understanding of ailments and thus improving chances of effective treatment. A 25 x 25 array has been used for segmentation in each of these cases. The current from the seed pixels have diffused in the array based on the connecting weights.This diffused current has pulled V_{seg} voltages of all the pixels either low or high. As can be seen from Figure 2 the objects of interest have been segmented successfully.

B. Pixel circuit layout

Figure 3 shows the layout for single pixel circuit. The area obtained for this circuit is 2.36 x 2.49 um^2. For an array of pixels, the same entity will be repeated multiple times. Hence the overall area of a large array can be estimated. In this work we have used 25 x 25 array which maps to 625 pixels and thus the overall area estimated is 3687 um^2.

C. Power consumption

As the circuit was implemented using 65 nm technology, the V_{dd} used for the ciruit is 1.2 V. The circuit operates in sub-threshold region and hence the operating current is of the order of nA. In this circuit (Figure 1), seeded pixels act as current source and this current diffuses in all other pixels. The current used in 25 x 25 pixel array for segmentation (Figure 2) is approximately 1 uA. Thus the power consumed by the system is 1.2 uW for 25 x 25 array.

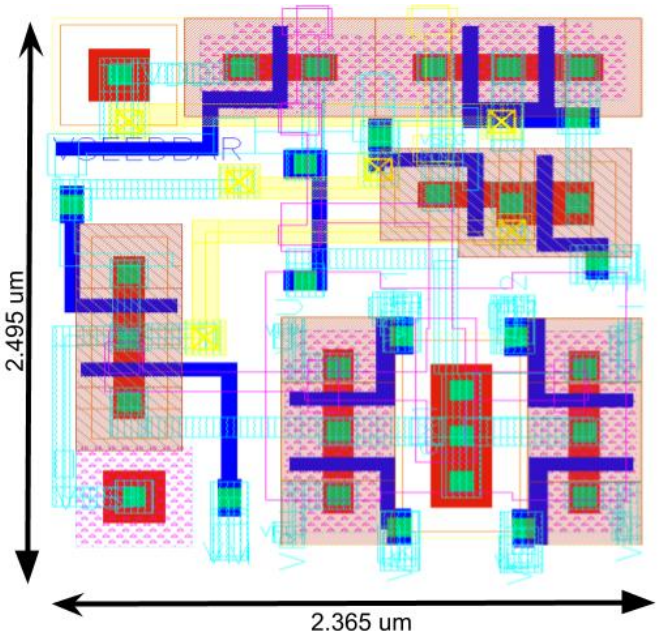


Fig. 3: Layout of a single pixel circuit

V. Conclusion

We have presented a low power semi-supervised real time image segmentation framework using analog circuits operating in sub threshold region of transistor. The problem is formulated based on the RW algorithm.

This analog array framework serves as a proof of concept and can be used to achieve multi label image segmentation, by changing the weights that are passed on to the array. Also, the weights computation can be modified based on different features other than intensity, based on applications. Analog array chip area is very less as compared to digital implementation and it ensures that this framework can be used in systems requiring small area and low power constraints. Due to very low power consumption, this system can be used effectively for applications such as intrusion surveillance. This work can also be used in image guided surgeries where real time image segmentation is a necessity. The analog array can be extended to three dimensions to incorporate segmentation for 3D images. In this case, each node will be connected to six neighboring nodes, with two nodes in each dimension. Proposed approach can effectively aid the implementation of graph-based computer vision algorithms on neuromorphic hardware for low power and real-time applications.

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