On-chip ESD Protection

High performance, low power dissipation and minimum area requirements are the driving forces for the scaling of modern semiconductor devices. Various devices like FinFET, III-V or SiGe based quantum well channel FinFET, Gate all around (GAA) or nanowire FET, Tunnel FETs, along with beyond CMOS solutions like Graphene FET (GFET) and Carbon Nano Tube (CNT FET) are projected to be the potential candidates for the emerging technology nodes. Although they provide superior scalability and improved performance, Electro- Static Discharge (ESD) reliability is foreseen as a serious challenge.

In the face of ever-growing demands for portable consumer electronics, flexible displays, low cost healthcare monitoring, and the like, researchers have looked upon the enormous solutions offered by flexible electronics. However, developing effective ESD handling strategies for these organic electronic devices is an ongoing research field.

Our research goal includes exploring the fundamental ESD behavior of these emerging technologies, establishing efficient ESD protection concepts and provide promising solutions for ESD robust designs.