RAMAN: A Re-configurable and Sparse tinyML Accelerator for Inference on Edge

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Abstract-Deep Neural Network (DNN) based inference at the edge is challenging as these compute, and data-intensive algorithms need to be implemented at low cost and low power while meeting the latency constraints of the target applications. Sparsity, in both activations and weights inherent to DNNs, is a key knob to leverage. In this paper, we present RAMAN, a Re-configurable and spArse tinyML Accelerator for infereNce on edge, architected to exploit the sparsity to reduce area (storage), power as well as latency. RAMAN can be configured to support a wide range of DNN topologies - consisting of different convolution layer types and a range of layer parameters (featuremap size and the number of channels). RAMAN can also be configured to support accuracy vs. power/latency tradeoffs using techniques deployed at compile-time and run-time. We present the salient features of the architecture, provide implementation results and compare the same with the state-of-the-art. RAMAN employs novel dataflow inspired by Gustavson's algorithm that has optimal input activation (IA) and output activation (OA) reuse to minimize memory access and the overall data movement cost. The dataflow allows RAMAN to locally reduce the partial sum (Psum) within a processing element array to eliminate the Psum writeback traffic. Additionally, we suggest a method to reduce peak activation memory by overlapping IA and OA on the same memory space, which can reduce storage requirements by up to 50%. RAMAN was implemented on a low-power and resource-constrained Efinix Ti60 FPGA with 37.2K LUTs and 8.6K register utilization. RAMAN processes all layers of the MobileNetV1 model at 98.47 GOp/s/W and the DS-CNN model at 79.68 GOp/s/W by leveraging both weight and activation sparsity.

Keywords—Convolutional neural networks (CNNs), deep learning, hardware acceleration, sparse processing.

I. INTRODUCTION

Deep neural networks (DNNs) have become ubiquitous in various cognition and learning problems [1]–[4]. DNNs are often computed in the cloud, and the inferred result is delivered back to an edge node, introducing delay owing to constrained communication bandwidth. Thus, the deployment of DNNs directly on edge has recently attracted more attention since it offers many inherent benefits, including privacy, bandwidth savings, and latency reductions. However, the computation on

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an edge device poses numerous challenges due to power, memory, and resource constraints. GPUs and CPUs conventionally used in cloud platforms are extremely power intensive and area inefficient and thus cannot be directly deployed on edge. A promising avenue to pursue in this respect is the development of an accelerator tailored for neural computations on edge. A customized hardware design for neural networks provides an opportunity to optimize dataflow, memory access and exploit network sparsity to overcome edge computing bottlenecks.

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Sparsity is an inherent attribute in most DNNs which can be leveraged on hardware. It is estimated that approximately 40% of the input activations (IAs) and 50% of weights (Ws) are sparse in the MobileNet model [5], [6] trained on the Imagenet dataset [1] with the hardware-aware pruning strategy presented in this paper. Other well-established networks like AlexNet [2], VGG-16 [7], and ResNet-50 [8] show similar sparsity statistics. Thus sparsity induces a lot of ineffectual zero computations that can be skipped. Aggressive pruning strategies can further reduce computations if a slight reduction in inference accuracy is acceptable. In this direction, several attempts have been made in the literature to maximize the sparsity by zeroing out low-magnitude weights [9]-[12]. In addition to weight sparsity, the commonly used rectified linear unit (ReLU) activation function clamps all negative activation values to zero, resulting in sparse output activations (OAs), which become IAs to the subsequent layer. Even though exploiting weight sparsity in hardware has been thoroughly investigated, leveraging activation sparsity in hardware efficiently is a topic of research and needs further exploration. This disparity is primarily because of the fact that it is possible to enforce structured sparsity in weights during training by pruning in a hardware-aware fashion (by knowing the underlying hardware architecture and the dataflow) that maximizes the overall hardware utilization and efficiency. However, the activation sparsity is unstructured and highly challenging to leverage on hardware as the data varies dynamically and depends on the environment [13].

A. Related Work

Early work in this domain used the indirection principle to exploit sparsity in one of the operands meaning in either weights or activations, but not both. Cnvlutin [14] exploits sparsity in IA by storing them in a compressed format as value and index pairs. The index information of the nonzero activations is used to perform in-direct memory access to extract dense weights. In another work, Cambricon-X [15]

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uses the same indirection principle, assuming sparse synaptic connections. The input neurons with non-zero synaptic connections are transferred to a computational unit to perform MAC (multiply-accumulate) operations. These architectures are inefficient as they are intended to exploit sparsity present in only one of the operands (W or IA). The dense processing core can quickly adapt to accommodate one operand sparsity by in-direct memory access.

EyerissV1 [16] is one of the early works investigating activation sparsity to save power by employing data-gating logic. When the IA is zero, the data gating logic disables the weight read from a local spad and prevents the MAC datapath from switching. Although this method improves energy efficiency, it does not reduce latency. EverissV2 [17] exploits sparsity further in both IA and W by preserving the data in compressed form all the way to the computational element and adopting a row stationary dataflow like EyerissV1. They employ a two-step search technique by retrieving non-zero activations and then utilizing the IA's channel index to fetch non-zero weights, requiring a deeper pipeline and complex processing element (PE) architecture. EyerissV2 employs an external DRAM for storing the activations and parameters and requires a complex hierarchical mesh network to route the data to different computational elements on-chip. We avoid such complexities in RAMAN as we target tinyML edge applications with all on-chip memory implementation.

Computer architects face two significant challenges in designing a sparse neural network accelerator leveraging both IA and W sparsity. First is the front-end challenge, where a sufficient number of non-zero IA and W pairs stored in a compressed format must be transferred to the computational unit to keep the MAC utilization high. Maintaining high MAC utilization is often tricky because it requires channel index matching to guarantee that the valid W-IA from the same channel is multiplied. Second, the back-end challenge where the partial-sum (Psum) addresses have to be aligned and immediately reduced within the computational element before a writeback. If the addresses are not aligned, then the Psums cannot be reduced, leading to significant writeback traffic and access contention. SCNN [18] and Sticker [19] try to overcome the front-end challenge; however, these works are plagued by the back-end problem. SCNN [18] uses channel-last dataflow to maximize the multiplier utilization at the cost of high output traffic and access contention. In the channel-last dataflow, the non-zero W and IA values are first organized in the pixel dimension, followed by the channel dimension in memory. Since any non-zero IA can be multiplied with any W in the same channel, it's easy to form non-zero W-IA pairs for computation resulting in high MAC utilization. However, this approach makes the Psum reduction (accumulation) highly challenging. As a result, the output writeback traffic is very high and requires a crossbar switch to arbitrate the data movement. Sticker [19] also uses channel-last dataflow and adopts a twoway set associative PEs to reduce memory access contention and collisions. However, since this strategy requires data reordering to prevent collisions, which are done offline using the CPU, it ultimately defeats the whole purpose of latency and energy reductions that sparsity offers. SNAP [20] is one of the latest DNN accelerators that tries to overcome the back-end problem by employing channel-first dataflow. Non-zero W and IA data are organized and processed in the channel dimension first and subsequently in the pixel dimension in the channelfirst dataflow. This ensures that the Psums calculated by the multiplier array are locally reduced before writeback, thus decreasing the writeback traffic. However, pairs of non-zero IA and W of matching channels have to be extracted, and they utilize address matching units (AMU) and sequence decoders to do the same. The AMU uses $N \times N$ comparators to match W and IA channel indices, making it highly inefficient as the area and power grow quadratically with N. EIE [21] exploits both IA and W sparsity but only supports fully connected (FC) layer making it incompatible to run convolution operations.

In addition, several FPGA-based implementations have been proposed in the literature [22]-[28]. NullHop [22] exploits the activation sparsity of the neurons in CNNs to accelerate the computation and reduce storage. However, this work does not exploit weight sparsity. Shah et al. [23] propose a run-time programmable coprocessor architecture to accelerate CNNs. However, programmability is limited to the standard convolution-type networks, and the sparsity optimizations have not been studied. McDanel et al. [24] propose a full-stack optimization framework to speed up CNNs by leveraging weight sparsity by column-combine strategy and reducing power by clock gating when activations are zero. Zhang et al. [25] and Nguyen et al. [26] propose CNN accelerators for YOLOv2 networks, and their architectures are hardwired to support a particular topology without any programming flexibility. Ma et al. [27], and Yu et al. [28] provide FPGA CNN implementations without exploiting sparsity and have limited programming capability.

B. Our Contributions

This work presents a re-configurable and sparse deep neural network accelerator that exploits both IA and W sparsity. To address the front-end challenge, we employ Gustavson's inspired dataflow [29] with the hardware-aware balanced weight pruning strategy to keep workload uniform across all the PEs and maintain high MAC utilization. The back-end issue is resolved by reducing Psum locally within a processing element (PE) array; this reduces the writeback bandwidth and eliminates memory access contention because only the final result is sent back to memory rather than every intermediate result.

Latest advancements in quantization techniques [30], [31] in DNNs have eliminated the need for floating-point arithmetic (during inference), and simple energy-efficient fixed-point arithmetic has proven adequate to achieve reasonable accuracy. Despite having a highly efficient computational realm, today's design has a memory bottleneck which is evident from [32]. Memory access (especially DRAM) is orders of magnitude more expensive than conventional arithmetic operations. The most state-of-the-art DNN accelerators, except for EIE, utilize an external DRAM to store IAs and Ws and pay the penalty of unprecedented memory access cost. Since our architecture is targeted at tinyML edge computing applications with stringent energy budgets, using external DRAM and paying high energy costs becomes untenable. Thus, in this work, we do away with the requirement for a DRAM and only use the on-chip SRAM to store the model weights and its activations. However, the memory size of the on-chip SRAM is limited due to area constraints, which necessitates model optimizations to fit modern networks such as MobileNets [5], [6] in SRAM. In this work, we introduce a hardware-aware pruning strategy to shrink the model size and intelligent memory scheduling to minimize peak activation memory to accommodate both model and activations on-chip.

Furthermore, prior works have limited flexibility regarding layers supported, and unsupported layers are often executed offline, making the overall system-level computation inefficient. This work supports a wide range of layer computations from the conventional CNN networks to the modern depthwise separable convolutions constituting depth-wise (DW) and point-wise (PW) layers. Our design also allows max pooling, average pooling, fully connected layers, and residual additions on-chip, eliminating the need to offload work to an external CPU. In summary, the following are the contributions and features of the RAMAN architecture presented in this paper:

- Memory Hierarchy: RAMAN employs a three-level memory hierarchy comprising low-cost levels such as reg-file (RF) and cache to amortize the data access cost to the high-cost on-chip global memory (GLB-MEM) (c.f. Section II-B). The reg-file is used for Psum reduction locally inside the PE to overcome the back-end challenges.
- Sparsity: RAMAN exploits both IA and W sparsity to achieve higher throughput and energy efficiency. Sparsity is leveraged in storage, computation and data movement. Input activations are stored in compressed form in a cache, and a simplified version of the compressed sparse row (CSR) format [33] is used for storing weights in both on-chip global memory and cache. Since RAMAN adopts a hardware-aware balanced pruning technique, it is not necessary to keep bounds/row index pointers, and thus we have further optimized the CSR format based on our requirements to minimize W storage (c.f. Section V of the supplementary document). In computation, sparsity is leveraged in two ways; for the layers with the maximum computational density (such as PW), RAMAN can skip the processing cycles with zero data, improving throughput and energy efficiency. However, skipping processing cycles won't reap any benefit in the layers with relatively low computational density (such as DW); in such cases, the design only data-gates the cycles with zero data but does not skip them. This strategy minimizes architectural complexity and improves overall energy efficiency. Finally, sparsity is utilized in data movement as only non-zero data is fetched and propagated in the network, lowering memory bandwidth and increasing energy efficiency even further.
- **Programmability:** RAMAN supports both traditional CNN models and modern separable convolutional models that constitute depth-wise and point-wise layers. In addition, it supports the execution of max pooling, average pooling, and fully connected layers. To enable this model and layer

flexibility, we propose a network-on-chip (NoC) that can adapt to a wide range of bandwidth requirements. It can provide a high bandwidth IA data from the cache to keep the PEs busy when there is limited IA reuse (for DW layers); when the IA reuse is high (in PW and FC layers), it reduces IA data bandwidth and increases W bandwidth. In addition, RAMAN offers an instruction memory and a dedicated instruction set to store and program different network topologies.

- **Dataflow:** RAMAN incorporates novel dataflow inspired by Gustavson's algorithm [29] to reduce memory access for the PW layer, which is the most computationally intensive layer. Additionally, the NoC is reconfigured to support weight stationary dataflow for DW and standard convolutional (CONV) layers. This hybrid dataflow architecture, enabled by dynamic NoC reconfiguration, maps the computation of a particular layer to its optimum dataflow to achieve maximum energy efficiency and minimum data movement cost.
- **Peak-Memory Reduction** The state-of-the-art accelerators logically partition the IAs and OAs inside the memory, where the total activation memory is the sum of IA and OA memory spaces. This logical partition is eliminated in our work, and the OAs are directly overwritten onto the IA memory space, lowering the peak activation memory requirements. RAMAN employs an intelligent memory scheduling scheme presented in Section III-A to prevent memory collision issues that ensue after removing the logical partition.
- Run-time Activation Pruning (RAP): RAMAN performs a hardware-aware activation pruning at run-time to increase the activation sparsity, and the architecture effectively leverages this strategy to increase throughput and energy efficiency. We believe this is the first attempt of its kind, and our offline experiments demonstrate the network's resilience to such pruning strategies. Section II-C provides a detailed description of RAP.
- Hardware-aware balanced weight pruning: We propose a hardware-aware balanced weight pruning strategy that reduces memory storage, access, and processing latency. The hardware-aware pruning is an example of software-hardware co-optimization, where a DNN is pruned during the training process, considering the underlying hardware architecture. By ensuring uniform zero/non-zero weight distribution across the weight tiles, the balanced pruning methodology solves the issue of workload imbalance. Without this strategy, non-zero weights would be unevenly distributed over different weight tiles processed by different PEs, resulting in workload imbalance, and the overall performance would be limited by the PE with the heaviest workload. The PEs with low non-zero weight tile distribution completes their execution sooner and must be stalled for the slower ones (the PEs with high non-zero weight tile distribution).
- Flexible quantization: RAMAN supports variable precision quantization of Ws and IAs supporting 2b, 4b, and 8b precisions. In addition, the architecture is programmable such that the precision of individual layers can vary to meet the required accuracy, storage, and latency target.

The rest of the paper is organized as follows: Section II presents the architecture of the RAMAN accelerator. The architectural features that make RAMAN feasible on edge are highlighted in the Section III. Section IV provides implementation results, and Section V concludes this article.

II. SYSTEM ARCHITECTURE

A. Top-Level Architecture

Fig. 1 shows the top-level architecture of the RAMAN accelerator system. The architecture can be broadly categorized into:



Fig. 1: Top-level architecture.

- **Compute:** The compute sub-system comprises a processing element (PE) array, an activation sparsity engine (ASE) and a post-processing module (PPM). The multiply and accumulate (MAC) operations are performed by 12 spatial PEs in the PE array, which are arranged in a 3x4 rectangle. The ASE leverages input activation sparsity to minimize latency and power by skipping ineffectual zero computations. The PPM performs ReLU, quantization, pooling, bias and residual addition operations. Sections II-C-II-E gives a detailed description of the PE array, ASE and post-processing module.
- Memory: The memory sub-system comprises an on-chip global memory (GLB-MEM), activation and parameter cache, and instruction memory. GLB-MEM stores the parameters of all layers and the input and output activations of a specific layer. Cache exploits temporal reuse in parameters and activations to reduce energy-expensive data access to the large on-chip GLB-MEM. We employ a three-level memory hierarchy composing GLB-MEM, cache and RFs (inside PEs). In addition, we have the instruction memory to store layer configuration instructions of individual layers. A detailed description of the GLB-MEM and cache is provided in Section II-B.
- **Control:** The control sub-system encompasses a top-level controller to coordinate: 1) data transfer between the GLB-MEM and cache; 2) traffic between the cache and PE array utilizing the NoC; 3) traffic between the PE array, PPM and GLB-MEM; 4) operations of the ASE, PE array, NoC, and PPM. We do not use a separate controller for each of the

12 PEs since they are all identical and operate in lockstep, meaning that their processing states are equivalent with regard to one another. The top-level controller is responsible for issuing the control signals to all the 12 PEs. A detailed description is provided in Section VI of the supplementary document.

B. Global and cache memory

The GLB-MEM comprises of activation and parameter memory banks. We overlay the input and output activations onto the same memory space, as discussed in Section III-A to minimize the activation memory storage. The parameter memory is 192b wide with a single port synchronous read/write interface, whereas the activation memory is 32b wide with dual address ports.

Cache enables temporal reuse of IA and W, minimizing the global memory accesses, which lower power consumption incurred in accessing global memory. The cache memory is a banked architecture comprising a set of 27 memory banks. Each bank is an 8b wide dual port synchronous read/write memory. Cache banks are dynamically partitioned based on the layer being executed. For instance, three banks are designated for activations in the PW layer, whereas twelve, four, and three banks are set aside for activations in the DW, FC, and CONV layers. W or IA are fetched directly from the GLB-MEM and processed in the PE array skipping cache when reuse is low. The global and cache memory block diagrams are shown in Fig. 8 of the supplementary document.

C. Activation sparsity Engine (ASE)

The activation sparsity engine serves two purposes. First, it reduces the cycles needed to write a block of data from the GLB-MEM to cache through ping-pong-based shift registers. Second, it aids in exploiting activation sparsity. Sparsity is leveraged in two ways: 1) by data gating the cycles with zero data and disabling the memory read to prevent the datapath from switching, thereby reducing dynamic power; 2) by skipping the processing cycles entirely to improve energy efficiency and throughput. IAs are routed through the ASE to record the position of zeros, and this information is utilized during computation to either gate or skip zero computation, depending on the layer under execution. The layers with low computing density (e.g., DW) adopt the gating strategy, and the layers with relatively high computational density (e.g., PW) employ the zero skipping technique in addition to data gating. This hybrid approach reduces architectural complexity since imposing zero skipping during DW execution has no positive impact on performance. The design details of the ASE are provided in Section II of the supplementary document.

Area overhead of the ASE in terms of LUTs (lookup tables), registers and memory utilization is insignificant, as demonstrated in Section IV.

1) ASE illustration: Fig. 3(a) illustrates the working of ASE for the PW layer. The three IA tiles are loaded into the shift register bank, and the non-zero detector module generates the bitmap. In Fig. 3(a), the second input channel of tile-2 is pruned as the value is less than the threshold value of



Fig. 2: Activation sparsity engine.



Fig. 3: (a) ASE Illustration for the PW layer. (b) Processing Element (Type-1).

20, inside the RAP block. The bitmap matrix is column-wise ORed to obtain the OR_BITS vector. The columns (2 and 3) are skipped during computation as all elements are zero post RAP. The channel indices (1 and 4) are cached in buffers 2 and 3, and they are subsequently utilized as addresses to retrieve the corresponding input channel weight from the cache during computation. Additionally, the column-wise bitmap is stored in buffer 1 for non-zero channel indices (1 and 4), which is accessible during computation cycles to activate or disable the

PE's data registers as depicted in the figure. In the example shown, for the first input channel, all the rows of the PE array are active as the bitmap is '111' for that particular column, and in the fourth channel, row-2 of the PE array is deactivated as the bitmap is '101'. Additionally, only the non-zero elements of the IA matrix are saved in cache banks utilizing the bitmap data. Just the bitmap is saved in buffers for other layers, not channel indices, as they only facilitate data gating and not cycle skipping.

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D. PE Array

The PE array comprises 12 processing elements spatially distributed along three rows and four columns. It is coupled with the Network-on-chip to route the data among different PEs.

1) Network-on-chip: The network-on-chip handles data delivery between the cache, the PE array, and between different PEs. The following are the NoC's responsibilities: 1) Support various data delivery patterns needed by different layers; 2) Provide sufficient data bandwidth for parallel processing to keep the PEs active and improve utilization; 3) Handle various strides and padding, and 4) Leverage spatial data reuse to increase energy efficiency.

To accomplish this, we employ a network of row and column routers. The column routers distribute a cached data block across four columns of the PE array, while the row router further splits the incoming packets and delivers input to the PE in a specific row. Furthermore, the output from the PEs is directed to the post-processing module via the row routers. Section II-F goes into greater detail on the various data delivery patterns to perform different layer computations.

2) Processing Element: Fig. 3(b) shows the architecture of the PE. We employ three types of PEs to support dataflow flexibility for different layer types. The architectures of the other two PE types constituting the last column of the PE array are presented in Figs. 10, 11 of the supplementary document. The fundamental elements of all PE configurations are an 8b multiplier, a 24b adder constituting MAC (Multiply and Accumulate Unit), and a reg-file. 8b W and IAs are provided as input and accumulated using the MAC unit, and a 24b Psum is saved in the RF. Offline experiments show that the Psum could fit within the 24b range. The type-2 and type-3 PEs use four-ported RF (4 input & output ports), while the RF in type-1 PE has four input and eight output ports, each with a width of 24b and a depth of 16. Thus, the RF can be addressed using 4b. The Psums are locally reduced inside the PE array, and the final result is written back to the memory after quantization in PPM, thereby reducing the writeback bandwidth and eliminating memory contention.

Power saving: PE implements data-gating logic to leverage zeros in the IAs for saving processing power in the layers

with low computational density, such as DW. The red-bordered registers in Fig. 3(b) are data-gated, and if a zero IA value is detected (provided by the bitmap bits stored in ASE buffers), then the gating registers are disabled to prevent the MAC datapath from switching.

SIMD support: PE supports SIMD processing, evident from Fig. 3(b), by performing four MAC operations per cycle, thereby speeding up the processing four times. In addition, SIMD processing also enables W and IA reuse, thereby reducing the number of memory accesses. RF has four write ports to simultaneously write the Psums from the four MAC units.

Variable precision: The PE datapath supports variable precision Ws and IAs. The reconfiguration of the data path for the 4b-W and 4b-IA using the same 8b datapath is shown in Fig. 3 (b). First, two 4b-Ws and 4b-IAs are packed as an input to the 8b multiplier to compute two 4b multiplications doubling the throughput. Next, the accumulator reduces the ensuing partial outputs (PO₁ and PO₂), each 8b wide. Similarly, for the 2b-W and 2b-IA case, the multiplier simultaneously does four 2b multiplications boosting throughput by 4x.

E. Post Processing Module

The post-processing module (PPM) is responsible for ReLU activation, bias addition, quantization, residual addition, max pooling, and average pooling operations. The PPM operations can broadly be categorized into memory pre-fetching, computation, and writeback stages. In the pre-fetching phase, the post-processing parameters such as bias (b), α , and β are pre-fetched from the GLB-MEM and cached locally in a 160b wide parameter buffer. α and β represent dyadic scaling parameters computed offline. The pre-fetching is overlapped with the PE array computations to amortize the memory access latency. In the computation phase, the Psum output obtained from the PE array is added with bias in sub-module (a) of Fig. 4. The result is then passed to the ReLU block that clamps the negative values. ReLU is implemented by a sign-bit (MSB) bit comparison. If the MSB bit is 0, the ReLU block outputs the input; else, it outputs a zero. The output of this block is a ReLU-activated Psum which is then quantized to obtain an 8b representation and written back to the memory. The



Fig. 4: Post-Processing Module.

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Fig. 5: Dataflow configuration across an array of PEs in RAMAN for (a) DW computation (b) PW computation and (c) FC computation.

quantization operation is performed in sub-module (c) of Fig. 4. The implementation detail of the quantization operation is provided in Section III of the supplementary document.

The same hardware can be reused to perform average pooling and max-pooling operations. For average pooling, the adder used for bias addition is re-purposed as an accumulator, and the parameter buffer is re-purposed to store the intermediate accumulation results. Division of the accumulated sum by HW (Height \times Width of the feature map) is performed in the sub-module (c) by expressing 1/HW in the dyadic form $\frac{\alpha}{2^{\beta}}$. An additional comparator is needed for max-pooling, as shown in sub-module (a). The PPM also supports residual input additions in sub-module (b).

PPM uses 4-way SIMD to improve throughput by performing 4 post-processing operations each cycle.

F. Dataflow

1) DW: DW layer uses a weight stationary systolic dataflow where the W remains static during the computation. IAs of dimension $(H_{in} \times W_{in} \times M)$ are partitioned into tiles of size $(1 \times W_{in} \times 4)$ and Ws of dimension $(3 \times 3 \times M)$ are partitioned into tiles of size $(3 \times 3 \times 4)$. Then three IA tiles are streamed from the cache to the PE array from top-to-bottom, and the Psum obtained is spatially reduced along the PE columns from left-to-right. A global accumulation is performed by the last column of PEs to obtain a final accumulated result. This mapping allows the reuse of IA along a column and Psums are spatially reduced inside the PE array. Since each PE supports SIMD with four MAC operations per cycle, four input IA channels are convolved with four W channels in every cycle. The systolic data flow necessitates proper synchronization of IA and Psums, as shown in Fig. 5(a). Each processing run generates a tile of OA of size $(1 \times W_{out} \times 4)$, and it takes $(H_{out} \times 1 \times M/4)$ runs to obtain all outputs. The dataflow also allows strided convolution and zero-padding. The CONV layer uses the same dataflow as the DW.

2) *PW*: The PW layer execution can be represented by 2D matrix multiplication of IA with dimension $(HW \times M)$ and weight W with dimension $(M \times N)$ to produce OA with dimension $(HW \times N)$ as shown in Fig. 5(b), where M and N are number of input and output channels respectively. The IA matrix is partitioned into HW tiles each sizing $(1 \times M)$, and the W matrix is partitioned into N/n tiles each sizing



Fig. 6: Illustration of the IA and OA memory space overlapping to reduce peak activation memory.

 $(M \times n)$. Since the PE array comprises 3×4 PEs, three IA tiles and four W tiles are passed to the PE array for computation in a single processing run. An IA tile is broadcasted to four PEs in a row, and a W tile is broadcasted to three PEs in a column. This mapping allows spatial reuse of IA along a row and W along a column. The Psums are locally accumulated and stored in the RF of individual PEs, and the final Psum is transferred to the PPM through row routers of NoC, reducing output writeback traffic to GLB-MEM. The IA and W tiles are sent to the PE array in compressed form for computation. In every processing run, $(3 \times 4n)$ tile of OA is generated, and it takes $(HW/3) \times (N/4n)$ runs to construct the entire OA matrix. n depends on the RF depth and is set to 16 in our implementation. This dataflow ensures the maximum reuse of IA and W with low OA writeback bandwidth.

3) FC: The FC layer can be represented by vector-matrix multiplication, as shown in Fig. 5(c). The IA is denoted as a vector of size $(1 \times M)$, and W is denoted as a matrix of size $(M \times N)$. The IA vector is divided into four tiles of size $(1 \times M/4)$, and each tile is broadcasted to three PEs in a column. The W matrix is divided into $4 \times N/6$ tiles of size $(M/4 \times 6)$ and is multicasted to three PEs in a column. A single PE receives two weights and a single activation per clock cycle and performs two MAC operations. The Psum reduction is made in two levels: PE-level and core-level. At the PE level, M/4 activations and $M/4 \times 2$ weights are streamed into each PE, and the resulting Psums are locally accumulated inside PE for M/4 cycles. At the core-level, the Psums stored in the RF of each PE are spatially reduced along four columns of the PE array. This two-level Psum reduction reduces the writeback traffic to GLB-MEM. The last column output provides the final result, which is sent to the PPM. Six OAs are generated in every processing run, and N/6 runs are required to construct the entire output vector. Each PE only uses two of the four MAC units available due to bandwidth constraints and lowweight reuse in the FC layer.

III. RAMAN MEMORY OPTIMIZATIONS TO SUPPORT DEPLOYMENT AT THE EDGE.

The RAMAN accelerator was developed targeting tinyML edge computing applications, and the following are the features that enable RAMAN to be deployable on edge:

A. Peak activation memory reduction:

The state-of-the-art (SOA) accelerators use two different memory spaces for storing IAs and OAs in a single memory. The IA and OA memory spaces are logically partitioned to prevent memory collision issue. This conventional approach requires a peak memory of:

$$MEM_size_{(SOA)} = max(\{sum(IA^l, OA^l)\}_{l=1}^L)$$
(1)

Where $MEM_size_{(SOA)}$ denotes the peak memory required by the state-of-the-art accelerators, L represents the total number of layers in the network, IA^l, OA^l represents the IA and OA memory sizes of a particular layer 'l'. Effectively in the conventional approach, the activation memory size is governed by the layer with the maximum sum of IA and OA memory sizes.

In our approach, as illustrated in Fig. 6, the logical partition between IA and OA memory spaces is eliminated, meaning that the OAs are overwritten in the same IA memory space. The memory size required by the proposed approach is given by:

$$MEM_size_{(RAMAN)} = max(\{max(IA^l, OA^l)\}_{l=1}^L) \quad (2)$$

Where $MEM_size_{(RAMAN)}$ denotes the peak memory required by RAMAN. Compared with the conventional approach, the proposed memory reduction scheme reduces the peak activation memory of the MobileNetV1[†] model trained for visual wake word (VWW) task by 37% and the DS-CNN[†] model trained for keyword spotting (KWS) application by 49% as shown in Fig. 6. We have made a couple of modifications to the original MobileNetV1 [5] and DS-CNN models [34] as per our requirements, and the modified models are denoted as MobileNetV1[†] and DS-CNN[†] models from here on.



Fig. 7: Comparison of dataflows in terms of memory accesses.

However, the memory collision issue arises while overwriting the OA into the IA memory space if the IA is not consumed before the OA writeback. This problem can be solved by storing a copy of the IA tile in the cache and then proceeding with the computation, as shown in Fig. 6. This makes the original copy of the IA tile (e.g., IA tile-1 in Fig. 6) in the GLB-MEM activation bank redundant, allowing the OA tile to occupy that space. The disparity in tile sizes between IA and OA is another challenge with the proposed approach. If the OA tile is larger than the IA tile, it might corrupt the contents of IA tile-2 by overflowing the memory area of IA tile-1 (cf. Fig. 6) and spilling over the subsequent tile (e.g., IA tile-2 in Fig. 6). This is particularly true in the PW layer when N>M, but it's not a concern in the DW layer because OA is always less than (if stride>1) or equal (if stride=1) to IA. Intelligent data organization inside the memory and pre-fetching the IA tile-2 to the cache prior to OA tile-1 writeback aids in resolving this issue.

B. Dataflow to reduce memory accesses:

Fig. 7 shows the GLB-MEM memory accesses evaluated for a single PE for different dataflows and their corresponding abstract loop nests. The analysis was carried out on the PW layers of the MobileNetV1[†] model [5], whose operation can be described as a matrix-multiplication of $IA_{(HW \times M)} \times W_{(M \times N)}$, where input channel M is a shared dimension of multiplication.

The output stationary (OS) dataflow, also termed inner product dataflow has the shared dimension in the innermost loop and achieves good output reuse (M times) but has poor input reuse. It computes an OA element one at a time by traversing a row of IA and a column of W. On the other hand, the Input stationary (IS) and the Weight stationary (WS) dataflows achieve good input reuse (N times) and weight reuse (HW times), respectively, but poor output reuse. It computes one partial output matrix (PO) of size ($HW \times N$) at a time by traversing a row of W and a column of IA in IS (or a column of W^T and a row of IA^T in WS) and M such matrices are generated before the final reduction. The size of the partial output matrix is massive to be stored locally inside the PE and thus has to be saved in the GLB-MEM, creating significant output data traffic evident from Fig. 7. Additionally, the bandwidth required by the partial output matrix (24b value) is much higher than the final output (8b value). Thus, moving the partial output matrix from PE to GLB-MEM is costly.

In this work, we employ a RAMAN dataflow (RD) inspired by Gustavson's algorithm to reduce the overall data-movement cost of the PW layer. It computes a row of 16 OAs at a time by traversing a row of IA, and a row of 16 elements from W. Since just 16 partial outputs are generated at a time, it is locally stored and reduced inside the PE. The dataflow is the most efficient as it avoids the two extremes of OS (by reusing IA by a factor of 16) and IS/WS (by eliminating the partial output traffic) dataflows. Only the quantized 8b accumulation result is sent to the GLB-MEM, drastically decreasing the output traffic. The W accesses from the GLB-MEM are reduced by storing a W tile in the cache and re-using them for HW times in the PW layer. Compared to the OS and IS/WS dataflows, the RAMAN dataflow significantly reduces the PW layer memory access by 1.9x and 6.5x, respectively.

IV. IMPLEMENTATION RESULTS

This section assesses the RAMAN's performance on Efinix FPGA [35].

A. Efinix FPGA Implementation Results

We evaluate RAMAN's performance on popular networks aimed at tinyML edge computing applications: MobileNetV1 and DS-CNN. The input dimensions are resized as per the requirement: 96×96 for the MobileNetV1[†] and 30×32 for the DS-CNN[†] model. The DS-CNN[†] model was trained on the google speech command dataset for the keyword spotting



Fig. 8: Leveraging sparsity in latency reduction: Compile-time and run-time latency vs. accuracy trade-off for MobileNetV1[†] model (left-panel) and DS-CNN[†] model (right-panel). Top-panel: Latency of RAMAN for different weight sparsity (pruning) ratios set at compile time. Bottom-panel: Latency distribution of PW layers in RAMAN with run-time activation pruning at different activation pruning thresholds (θ) with accuracy highlighted. The accuracy and latency estimates are for two tasks: keyword spotting using the DS-CNN[†] model trained on the Google speech command dataset and image classification using the MobileNetV1[†] model trained on the VWW dataset.

(KWS) application [36]. The input audio with each 1s duration was sampled at 16KHz and fed to the cascade of asymmetric resonators [37] to generate a cochleagram. RAMAN used the output cochleagram of size 30×32 as an input to infer the keyword. The MobileNetV1[†] model was trained on the Visual Wake Words (VWW) dataset [38] with input image converted to gray-scale. The specific MobileNetV1[†] and DS-CNN[†] network architectures deployed on RAMAN are provided in Section IX of the supplementary document.

RAMAN was implemented on an Efinix Ti60 FPGA, with parameters, instructions, and pre-processed inputs written into corresponding memories. The specifications of the RAMAN architecture are shown in Table I. The LUT breakdown of the RAMAN architecture is shown in Fig. 9(a). It is evident that the controller and the PE array consume most of the LUTs in FPGA fabric, accounting for 86% of LUTs, and the ASE utilization is insignificant. Fig. 9(b) shows the register breakdown of the RAMAN architecture. The PE array utilizes 52% of the registers since each PE comprises $16 \times 24b$ RF to store Psums. RAMAN provides the flexibility to downsize the PE RF width to 20b (or lower) depending on the application to reduce register utilization. The PPM stores post-processing parameters in registers leading to 32% register utilization. The LUTs and registers are inferred as the eXchangeable Logic and Routing (XLR) cells in Efinix FPGA.

The RAMAN architecture comprises 48 MAC units operating at 75 MHz, which theoretically translates to a throughput of 7.2 GOp/s. However, since operations involving zero are skipped in the PW layer, we achieve an effective throughput of 13.5 GOp/s and 10.5 GOp/s for the MobileNetV1^{\dagger} and DS-CNN[†] models, respectively by exploiting both activation and weight sparsity. The power consumption of the RAMAN architecture on Efinix Ti60 FPGA is estimated to be 136.96 mW (89.37 mW dynamic power + 47.6 mW static power) and 131.77 mW (84.39 mW dynamic power + 47.38 mW static power) for the MobileNetV1[†] and DS-CNN[†] models, respectively. Therefore, the effective power efficiency of RAMAN at 75 MHz and 75% PW weight sparsity is 98.4 GOp/s/W (or equivalently 2355 Inferences/J) for the MobileNetV1[†] and 79.68 GOp/s/W (or equivalently 6609 Inferences/J) for the DS-CNN[†] model. The power and memory breakdown of the RAMAN architecture is provided in Section X of the supplementary document.

The average MAC utilization of the DW and PW layers is around 59% and 86%, respectively, with overall utilization of

TABLE I: RAMAN Specificati	ons.
----------------------------	------

Platform	Efinix Ti60		
	CONV DW PW		
Layers Supported	EC and Max/Average pooling		
	Te and Max/Average pooring.		
Number of PEs	12 (4 MACs/PE)		
Reg-file Memory	PE Array: 0.576 KB		
	PPM: 0.32 KB		
Clock Rate	75 MHz		
Anithmatia Dreakian	W & IAs: 2b, 4b or 8b fixed point,		
Allumeuc riecision	Psums: 24b fixed point.		
Derman	137 mW for MobileNetV1 [†]		
Power	132 mW for DS-CNN ^{\dagger}		
XLR cells	52261 (85.96% util.)		
DSPs	61 (38.12% util.)		
Momory Ploaks	168 (65.62% util.) for MobileNetV1 †		
Wiemory Diocks	118 (46.09% util.) for DS-CNN ^{\dagger}		
Theoretical Throughput	7.2 GOp/s (3.6 GMACS)		
Effection Theory-hand	13.5 GOp/s for MobileNetV1 [†]		
Effective Inroughput	10.5 GOp/s for DS-CNN [†]		
Enorgy Efficiency	2355 Inferences/J for MobileNetV1 [†]		
Energy Efficiency	6609 Inferences/J for DS-CNN [†]		

78%. DW layers have a lower MAC utilization due to limited IA re-use and the time spent to fetch the IAs and Ws from the GLB-MEM memory. On the other hand, memory access latency of the PW layers in RAMAN is completely hidden with MAC operations; however, the latency introduced due to data fetch from the RF of PEs cannot be completely hidden as the next tile's MAC operation can be started only after completely evicting the contents of the RF of the current tile. The MAC units remain idle while fetching the contents of RF and transferring them to the post-processing module. This problem can be solved by double buffering the reg-file in the PEs, increasing the PW layer utilization to 97%.

B. Sparsity Results

1) Leveraging sparsity in latency reduction: Fig. 8 shows the accuracy vs. latency trade-off at compile-time and runtime. Figs. 8(a) and 8(b) demonstrate the RAMAN processing latency and model accuracy as a function of weight sparsity for the MobileNetV1^{\dagger} and DS-CNN^{\dagger} models, respectively. The required degree of weight sparsity is pre-set at compile time using the hardware-aware balanced weight pruning technique described in Section V of the supplementary document. The performance is assessed for four weight sparsity levels. It is evident that the latency reduction is almost linear with the degree of weight sparsity, and the accuracy degradation is minimal. Additionally, the latency distribution for the PW layers of the MobileNetV1[†] and DS-CNN[†] models are shown in Figs.8(c) and 8(d). There is a significant reduction in latency by leveraging IA sparsity. The latency gains are substantial in the final layers of the MobileNetV1[†] model due to an increase in IA sparsity and number of operations. In contrast, the DS- CNN^{\dagger} model is computationally intensive in the initial layers. Furthermore, we compare the latency after run-time activation pruning for different thresholds. Thresholds are set based on the input data distribution. For the MobileNetV1[†] model, RAP

with pruning threshold 40 reduces latency by an additional 16% compared to no pruning case, with accuracy degradation of $\approx 2\%$. For the DS-CNN[†] model, RAP reduces total latency by 12% with the pruning threshold set at 20. However, the possibility of minimizing latency with RAP is only confined to the initial layers since the final layers of DS-CNN[†] have low computational intensity.

2) Leveraging sparsity in memory access reduction: Table II shows the activation cache access breakdown for different layer types of the MobileNetV1[†] and DS-CNN[†] models. It is evident from the table that the majority of the cache accesses happen in the DW-PW layers, and the activation cache reads are more than the cache writes, leading to effective cache reuse. Additionally, leveraging IA sparsity reduces the cache accesses by 40 - 45%. Finally, Table III presents the weight cache access breakdown for different sparsity or pruning ratios. Again, a similar trend is observed where reads dominate writes, indicating effective cache reuse and the cache accesses reduce with increased sparsity ratio. In addition, it is observed that the weight cache reads are further reduced by 30% with IA sparsity since when the IA value is zero, the corresponding weight is not read from memory. However, the weight cache writes remain the same since all weight values are loaded to the cache initially, irrespective of IA sparsity. In addition, runtime activation pruning reduces IA cache access by 8 - 10%, and parameter cache reads by 13 - 21%.

TABLE II: Activation cache access breakdown for (a) DS-CNN^{\dagger} and (b) MobileNetV1^{\dagger} model.

	With	IA spa	rsity (ir	Without IA sparsity (in KB)				
Layer	Re	ad	W	rite	Re	ad	W	rite
	(a)	(b)	(a)	(b)	(a)	(b)	(a)	(b)
CONV	0.5	9.8	0.2	6.7	2.7	13.5	0.96	9.2
DW	171	356	77	144	281	630	129	246
PW	47	173	47	173	76	335	76	335
Pool	0	0	0	0	0	0	0	0
FC	0.13	0.26	0.06	0.26	0.13	0.26	0.06	0.26
Total	219	539	124	323	360	979	206	590

TABLE III: Weight cache access breakdown for (a) DS-CNN^{\dagger} and (b) MobileNetV1^{\dagger} model.

Weight		Read	Write (in KB)				
Sparsity	With 1	With IA sparsity		ut IA sparsity	-		
Sparsity	(a)	(b)	(a)	(b)	(a)	(b)	
0%	1727	6344	2451	9425	49	295	
25%	1295	4908	1839	7250	37	222	
50%	863	3472	1226	5075	25	149	
75%	432	2036	613	2900	12	76	

3) Leveraging sparsity in storage reduction: The global memory requirements of the design are tabulated in Table IV. The peak activation memory needed is obtained by overwriting OAs in the same IA memory space. The parameter memory needed is the sum of memory needed to store weights and post-processing parameters of all the layers. Taking pruning into account, the parameter memory reduces with an increase in pruning percentage, as shown in



Fig. 9: Resource utilization breakdown of (a) LUTs and (b) Registers.

Table IV.

TABLE IV: Global memory requirements.

Memory (in KB)	Activation	arameter N lifferent pr	ameter Memory with erent pruning ratios		
(III KD)	wiemory	0	0.25	0.5	0.75
DS-CNN [†]	54.72	61.968	49.656	37.392	25.104
Mobile -NetV1 [†]	44.56	324.288	251.328	178.368	105.384

C. Comparison with prior works

We compare RAMAN with other state-of-the-art (SOA) implementations in Table V. While most SOA accelerators support just CONV, RAMAN supports a wide range of DNN topologies, including CONV (standard convolutions), DW + PW (separable convolutions), FC, max and average pooling layers. RAMAN supports variable precision quantization of IAs and Ws. Unlike other SOA implementations, which use both on-chip and off-chip memories, RAMAN, being a tinyML edge accelerator, exclusively employs an on-chip memory to store activations and weights.

RAMAN's resource utilization and power efficiency are significantly better than other prior implementations making it an ideal candidate for resource-constrained edge devices. Table V also compares the architectural features regarding sparsity, peak-memory reduction and programmability. Very few works in the literature leverage sparsity in their design. NullHop [22] presents an architecture that exploits activation sparsity to accelerate computation (by zero skipping) and reduce storage requirements. However, the architecture doesn't exploit weight sparsity. McDanel et al. [24] present a method to exploit weight sparsity in the systolic arrays by a columncombining scheme that packs the sparse non-zero weights into a denser format. The activation sparsity is leveraged by clock-gating the logic when the activation is zero to save power. However, this method won't save computation cycles and memory accesses like in RAMAN. Unlike other prior implementations shown in Table V, RAMAN co-optimizes the software and hardware stack by training the model based on the underlying accelerator constraints. Hardware-aware pruning is one such optimization vector, where the network is pruned to reduce the workload imbalance of different PEs and improve utilization. Additionally, RAMAN performs runtime activation pruning and peak-activation memory reduction to make it compatible with tinyML edge applications which none of the other implementation support. Furthermore, most prior implementations are limited to standard convolution layers, and the unsupported ones are processed off-chip. In contrast, our design can support different network topologies eliminating the off-chip computation or FPGA reconfiguration.

V. CONCLUSIONS

Deep neural networks (DNNs) introduce weight and activation sparsity, enabling deep learning applications to operate more efficiently on hardware platforms with constrained resources and energy. However, these sparse models need specialized hardware architectures to fully benefit from the sparsity for storage, latency, and energy gains. In this work, a reconfigurable and sparse neural network accelerator exploiting both weight and activation sparsity is proposed. RAMAN uses an activation sparsity engine to leverage unstructured activation sparsity and a hardware-aware balanced pruning to exploit structured weight sparsity. We propose a novel dataflow inspired by Gustavson's algorithm that enables the Psum reduction with the PE array and significantly reduces the writeback traffic. The dataflow reduces the PW layer memory accesses by 1.9x compared to output stationary dataflow and 6.5x compared to input/weight stationary dataflow. Furthermore, we propose a technique to lower peak memory activation by overlaying IA and OA on the same memory space, which can reduce storage requirements by up to 50%. These memory optimizations in terms of memory accesses and memory storage enable RAMAN to be deployable on edge with a small form factor.

RAMAN supports a wide range of DNN topologies from standard CNN layers to modern DS-CNNs and can be configured to support accuracy vs. power/latency tradeoffs using techniques deployed at compile time and run time. RAMAN architecture was implemented on Efinix FPGA with 37.2K LUTs using 48 MAC units distributed across 3×4 PEs. The design achieves an overall energy efficiency of 2355 and 6609 Inference/J for MobileNetV1[†] and DS-CNN[†] models at 75 MHz on Efinix FPGA. The effective power efficiency

	NullHop	Shah et al.	McDanel et al.	Zhang et al.	Nguyen et al.	Ma et al.	Yu et al.	RAMAN
	[22]	[23]	[24]	[25]	[26]	[27]	[28]	(This work)
Distform	Xilinx	Xilinx	Xilinx	Xilinx	Xilinx	Intel Arria	Xilinx	Efinix
r latioi lii	Zynq-7100	Virtex-7	Virtex-7	Zynq-7000	Virtex-7	10 GX	Kintex-7	Ti60
Layers	CONV	CONV	CONV+	CONV	CONV	CONV+	CONV+	CONV+DW+
Supported	CONV	CONV	PW+FC	CONV	CONV	Pool+FC	Pool+FC	PW+Pool+FC
Num. of	128	1024	N/A	288	N/A	3136	1024	18
Mults	120	1024	IN/A	200	IN/A	5150	1024	40
Precision	16b	18b	N/A	8b	W:1b & IA:6b	16b	8b	2, 4 or 8b
LUTs	229k	78.32k	239k	83.24k	86k	138k [§]	94.76k	37.2k
Registers	107k	96.93k	201k	109k	60k	N/A	150.85k	8.6k
DSPs	128	1034	112	192	168	1518	516	61
Frequency (MHz)	60	150	170	200	200	200	200	75
Power Efficiency	27.4	7.2	N/A	19.71	52 20	NI/A	21.45	09 47*
(GOp/s/W)	27.4	1.2	IN/A	16./1	55.29	IN/A	21.43	98.47
Leveraging	Yes (Zero-	No	Yes (Clock-	No	No	No	No	Yes (Zero-
Act. Sparsity	skipping)	NO	gating)	NO	NO	NO	NO	skipping & gating)
Leveraging	No	No	Ves	No	No	No	No	Vos
Weight Sparsity	110	110	103	110	110	110	110	105
Hardware-Aware	No	No	No	No	No	No	No	Ves
Pruning	110	110	110	110	110	110	110	103
Run-time	No	No	No	No	No	No	No	Ves
Act. Pruning	110	110	110	110	110	110	110	105
Peak Act.	No	No	No	No	No	No	No	Ves
Mem. Reduction	110	110	110	110	110	110	110	103
Variable Precision	No	No	No	No	No	No	No	Yes
Run-time	Limited to	Limited to	Limited	No¶	No¶	Limited	Limited	Ves
Programmability	CONV	CONV	Linned		110	Linned		105

TABLE V: Comparison with the state-of-the-art (SOA) FPGA implementations.

[¶]The architecture is limited to YOLOv2 implementation.

[§]For Intel FPGA (Logic elements/ALMs).

*Estimated for 8b precision.

Run-time programmability means that the accelerator can support different network topologies without reconfiguring FPGA or synthesizing the design again.

of the system is estimated to be 98.4 and 79.68 GOp/s/W for MobileNetV1[†] and DS-CNN[†] models, respectively. A demonstration video of the proposed RAMAN accelerator on the Efinix Ti60 FPGA board for the keyword spotting task, where we control the maze game using the keywords uttered by the user, can be found here https://youtu.be/sCksj7nlBY8.

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RAMAN: Supplementary Material

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I. CNN BASICS

The CNN algorithm is built by stacking many computation layers for feature extraction and classification. CNN layers apply filters to an input feature map to extract embedded features and generate an output feature map as shown in Fig. 1. By constructing a very deep hierarchy of layers, modern CNNs achieve significantly higher accuracy by transforming the input image data into highly abstract representations known as feature maps. The computation of a layer in CNN is defined by:

$$\mathbf{OA}_{n,x,y} = ReLU\left(\mathbf{b}_n + \sum_{m=0}^{M-1} \sum_{i=0}^{K-1} \sum_{j=0}^{K-1} \mathbf{IA}_{m,x+i,y+i} \right)$$
(1)
$$\cdot \mathbf{W}_{n,m,i,j}$$

Where H/W is the height and width of the input feature map denoted as IA, H'/W' is the height and width of the output feature map denoted as OA. M is the number of input channels, and N is the number of filters or output channels. W denotes the weight and K denotes the filter height and width. A rectified linear unit (ReLU) activation function is applied to introduce non-linearity. The computational cost of the convolution is:

$$K \cdot K \cdot M \cdot N \cdot H \cdot W \tag{2}$$

CNN computation can be divided into two phases: 1) Training- where parameters are trained by observing a vast amount of training examples, and 2) Inference- where the network is deployed in the field with the trained parameters. Training is performed on the cloud on GPUs, and inference depends on the application and can employ GPUs, CPUs, MCUs, or customized neural network accelerators. For edge applications with limited area and power budget, customized neural network accelerators are preferred. However, DNNs require millions of operations even during inference, necessitating software and hardware optimizations to be deployable on edge. One such network architecture that seeks to minimize the number of operations is depth-wise separable convolutions (DS-CNNs), rendering it ideal for deployment on the edge.

The DS-CNN splits the convolution process into a pointwise and a depth-wise convolution. The depth-wise convolution applies a single filter for every input channel to capture the spatial information as shown in Fig. 2(a). In the point-wise convolution, we apply a 1x1 filter to combine the output of the depth-wise convolution as shown in Fig. 2(b). A standard convolution filters and combines in a single step, whereas the DS-CNN does the same in two stages. As a result, the model size and computation are reduced substantially, which is ideal for tinyML edge applications.

Depth-wise convolution with one filter per input channel can be written as:

$$\mathbf{OA}_{x,y,m} = \sum_{i=0}^{K-1} \sum_{j=0}^{K-1} \mathbf{W}_{i,j,m} \cdot \mathbf{IA}_{x+i,y+j,m}$$
(3)

where **W** is the depth-wise convolutional kernel of size $K \times K \times M$ where the m_{th} filter in **W** is applied to the m_{th} channel in **IA** to produce the m_{th} channel of the filtered output feature map **OA**.

Depth-wise convolution has the computational cost of:

$$K \cdot K \cdot M \cdot H \cdot W \tag{4}$$

The sum of depth-wise and 1×1 point-wise convolutions cost:

$$K \cdot K \cdot M \cdot H \cdot W + M \cdot N \cdot H \cdot W \tag{5}$$

By expressing standard convolution as depth-wise separable convolution, we get a reduction in the computation by:

$$\frac{K \cdot K \cdot M \cdot H \cdot W + M \cdot N \cdot H \cdot W}{K \cdot K \cdot M \cdot N \cdot H \cdot W}$$
$$\frac{1}{N} + \frac{1}{K \cdot K}$$

Thus, the DS-CNN model inherently reduces the number of operations carried out during inference.

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II. ACTIVATION SPARSITY ENGINE DESIGN

The ASE consists of five major blocks, as shown in Fig. 3.

- Shift Register Bank: Consists of six parallel shift registers (SRs), with even and odd SR pairs ping-ponging to minimize the time required to write a block of data from the GLB-MEM to cache. To begin with, all even SRs are in input mode, while all odd SRs are in shift/output mode, and the functionality is inverted in the following epoch. In the input mode, we load 32b activations parallelly into four registers of a SR. In the output/shift mode, 8b data is serially shifted into the non-zero detector block.
- **Ping-Pong Enable Logic:** Comprises a counter and 2:4 decoder to activate appropriate SRs in the shift register bank. The contents of the SRs are shifted when the *shift* control signal is asserted.
- Non-Zero Detector: The IAs read from the shift register bank are compared with zero to generate bitmap (b_0 to b_2 , B_3), which is 1 when the IA value is not equal to 0



Fig. 1: Computation of a CNN layer.



Fig. 2: DS-CNN computation of a layer. (a) Depth-wise (DW) computation, and (b) Point-wise (PW) computation.

and 0 otherwise, thus recording the position of zeros. The bitmap bits $(b_0 \text{ to } b_2)$ are sent to the run-time activation pruning (RAP) logic to perform activation pruning and generate a new set of bitmap bits $(B_0 \text{ to } B_2)$. Then the bits $(B_0 \text{ to } B_2)$ obtained from RAP are 'OR'ed to generate OR_BIT , which is required for zero skipping in the PW layer. The bitmap bits, along with the OR_BIT , are fed to the succeeding bitmap and non-zero channel index buffer module.

• Run-time Activation Pruning (RAP): As the name suggests, the RAP performs activation pruning during inference to improve the throughput and minimize computation latency. In our implementation, IA in the PW layer is tiled with each sizing $1 \times M$, and three rows of the PE array simultaneously process three such tiles, i.e., $3 \times M$ block of IA is processed in a single epoch. However, if all activations

in a column of $3 \times M$ block are zeros, that particular input channel or column is skipped entirely during the computation. Suppose there is only one non-zero activation in a column and the rest are 0; that activation value is pruned if it's below the predetermined threshold (θ) so that the column may be skipped during processing. The threshold value is precomputed during the training phase based on the input and hidden layers activation distribution. A pseudocode of the RAP logic is shown in Fig. 3. When any one of the bitmap bits $(b_0 \text{ to } b_2)$ is 1, and the remaining are 0s, then the activation values $(a_0 \text{ to } a_2)$ are compared with the threshold. If the value a_k is lesser than the threshold, then the corresponding bitmap bit B_k is made 0. If a column has more than one non-zero element, then the input bitmap bits to the RAP (b_0 to b_2) are retained. RAP improves the throughput by $\approx (10 - 15)\%$, and offers accuracy vs



Fig. 3: Activation sparsity engine.

energy/latency tradeoff which can be configured at run-time.

• Bitmap and non-zero channel index buffer: It consists of three buffers and a channel counter. When the *OR_BIT* is 1 in the PW layer, we save the corresponding input channel number obtained from the channel counter in the buffer. This information is useful during the computation as we perform computation only on input channels recorded in the buffer and skip the rest. In other layers (such as DW and CONV), we store the bitmap bits in buffers, which are later used to enable/disable the appropriate data gating registers in PEs (c.f Fig. 9-11).

The IAs are stored in a compressed format in the cache using the five blocks discussed above. The bitmap bits and the input channel numbers saved in buffers aid in power saving through data-gating and latency reduction through cycle skipping.

III. QUANTIZATION OPERATION IN POST-PROCESSING MODULE

The quantization scheme is derived from [1] and can be represented by the following equation:

$$Q(x) = round(\frac{\alpha \times x}{2^{\beta}}) \tag{6}$$

Where Q is the quantized representation of input x, α and β represent dyadic scaling parameters computed offline.

The rounding operation can be mimicked in a hardwarefriendly way as follows:

$$round(\frac{\alpha \times x}{2^{\beta}}) \approx floor\left(\frac{\alpha \times (x) + 2^{\beta-1}}{2^{\beta}}\right)$$
 (7)

Dyadic scaling ensures that α and β are fixed point integers; hence, the multiplication and division operations in Eqn. 7 can be efficiently implemented using an integer (fixed point) multiplier and a shifter. From offline accuracy analysis, scales α and β are set to 8b. Rounding operation can be visualized as adding 0.5, which is $\frac{1}{2^1}$ to the ReLU activated output. This can be thought of adding 1 left shifted by $\beta - 1$ times to the ReLU activated outputs, and then right shifting it β times. Post rounding, the result is clamped within the 8b range (-128 to +127 for 8b signed and 0 to 255 for 8b unsigned). In addition, if the ReLU output is zero, the downstream computations are disabled by data-gating registers to improve energy efficiency.

IV. INTRA-LAYER PIPELINING

Maintaining high MAC utilization is crucial for sustaining low latency and high throughput. This can be accomplished by pipelining the operations of a certain layer, as shown in Fig 4. Ld mnemonic denotes the memory access from the GLB-MEM; PW mnemonic indicates the point-wise operation of an IA tile with a W tile in the PE array; Rd denotes transferring the contents of RF from PE to PPM after the final accumulation, PP denotes post-processing, and Wb represents the final writeback of OA after ReLU and quantization inside the PPM, to the GLB-MEM. The IA and W can be loaded into the cache concurrently since there are separate activation and parameter memory banks. After the data tile is loaded into the cache, the PE array starts the MAC computation, and the final accumulated output is sent to the PPM. The data fetch from the PE RF, PPM operation, and final output writeback is





Fig. 4: PW layer timing diagram. $Ld_{(GM \to CB)}$ denotes memory transfer from the GLB-MEM to cache, $Ld_{(GM \to PPB)}$ denotes memory transfer from the GLB-MEM to the post-processing module buffer, PW_{PE} denotes the point-wise layer computation inside the PE array, $Rd_{(RF \to PPM)}$ represents moving Psum from RF inside PE to the post-processing module, PP_{PPM} denotes the post-processing operation, and $Wb_{(PPM \to GM)}$ denotes writeback of the final quantized output to the GLB-MEM. Computation and memory transfers are overlapped to minimize delay and improve MAC utilization. Δ represents post-processing parameters bias (b), α , and β .

pipelined. Furthermore, the Ld operation of the next IA and/or W tiles overlaps with the PW computation of the previous tile to amortize the GLB-MEM access latency. Since activation load (next tile) and store (last tile) can happen simultaneously, the activation bank is a dual address ported memory. Here we show the timing diagram of the PW layer as it is the most computationally intensive layer. Other layers in the network, such as DW and CONV, employ the same pipelining principle. The overall MAC utilization across the PW layers is 86% for the MobileNetV1[†] model.

V. HARDWARE-AWARE BALANCED WEIGHT PRUNING

We propose a hardware-aware balanced weight pruning technique to reduce memory storage and access and improve energy efficiency and throughput for the PW layer. The pruning is done during the training stage in an iterative manner to have minimum accuracy degradation [2]. Initially, the weights are divided into tiles of size $M \times n$ as shown in Fig. 5(a), and for ease of explanation, we have considered n = 4. A fixed number of weights are pruned in each tile row based on the magnitude, leading to structured sparsity, which can be efficiently exploited in our hardware. We employ the CSR scheme with modifications to store W in compressed form. The CSR scheme uses a set of non-zero values, bounds/row pointer, and index/column pointer to represent compressed information. The bounds/row pointer determines the number of non-zero elements present in a row of the sparse matrix, and the index provides the column index of the non-zero value. In our pruning scheme, since all the rows in a sparse matrix tile have the same number of non-zero elements, we don't have to store bounds explicitly. It further eliminates the PE workload imbalance problem, and the start location of a particular tile in memory can be easily identified. The index in our implementation provides a non-zero column index for a specific tile and not the entire sparse matrix requiring $log_2(n)$ bits instead of $log_2(N)$ in the conventional CSR approach. In our implementation, n is 16, requiring a 4b index, and the values of the weights are quantized to 8b. Thus, each non-zero weight element is represented by a 12b value-index pair.

The balanced pruning methodology ensures uniform zero/non-zero weight distribution across the weight tiles, thereby eliminating the workload imbalance problem. Without the balanced pruning strategy, the non-zero weights would be non-uniformly distributed across different weight tiles processed by different PEs resulting in workload imbalance, and the overall performance is limited by the PE with the heaviest workload. The PEs with low non-zero weight tile distribution completes their execution faster and has to be stalled for the slowest one (the PE with high non-zero weight tile distribution).

Fig. 5(b) shows the balanced weight pruning strategy employed in RAMAN with n = 16 for different pruning ratios.



(b)

Fig. 5: Hardware-aware balanced weight pruning illustration. (a) Decomposing a sparse weight matrix into a compressed dense matrix containing only non-zero elements and an index matrix. (b) Balanced pruning strategy for different pruning ratios.



Fig. 6: Top-level controller

VI. TOP-LEVEL CONTROLLER IMPLEMENTATION

The top-level controller employs a master-slave hierarchy to implement a layer execution. The slave controller carries out instruction execution, whereas the master controller is in charge of fetching and decoding instructions. In the instruction fetch stage, a layer-specific instruction scheduled for execution is fetched from the instruction memory and sent to the toplevel master controller. In the instruction decode stage, the fetched instruction is subsequently decoded to retrieve the opcode and layer configuration data. Control is then handed to the slave controller based on the opcode of a given instruction, which activates one of the five slave controllers according to the layer type specified by the opcode. Following the instruction execution, the master controller is activated to repeat the instruction fetch, decode and execute stages for the next instruction.

A RAMAN instruction is 80 bits wide as shown in Fig. 7, with a 3b opcode, and the rest of the bits are dedicated to storing the information related to each layer, like the zero pad, stride, IA dimension, channel dimension, etc.

VII. GLOBAL AND CACHE MEMORY

The global and cache memory block diagrams are shown in Fig. 8. A description of the architecture is provided in the main document.

VIII. PROCESSING ELEMENT

The detailed architectures of the processing elements of type-1 to type-3 are shown in Figs. 9-11. A description of

			80)b		
• • •	Stride	Zero Pad	IA tiles (K), W tiles (P)	FMAP Dim. (H,W)	Channel Dim. (M,N)	OPCODE
						3b

Fig. 7: An illustration of an instruction.



Fig. 8: Memory blocks of RAMAN: (a) Global Memory and (b) Activation and parameter cache.



Fig. 9: Processing Element (Type-1)



Fig. 10: Processing Element (Type-2)



Fig. 11: Processing Element (Type-3)

the PE architecture is provided in the main document.

IX. DATASET AND MODEL STATISTICS

We employ RAMAN for auditory and computer vision (CV) tasks. The dataset used for the auditory task is the Speech Command dataset [3] for Keyword spotting (KWS) application. The dataset is a collection of one-second utterances of simple keywords. The DS-CNN^{\dagger} model shown in Table II(a) is trained on the dataset for 12 classes as listed in Table I(a).

The dataset used for the CV task is the Visual Wake Word (VWW) dataset [4] for person/no-person detection in an image. The dataset is a set of 224×224 RGB images which are down-sampled to 96×96 and converted to grey-scaled for hardware deployment. The VWW dataset is used to train MobileNetV1[†] model shown in Table II(b) with two classes listed in Table I(b).

The model statistics of the targeted applications that gave maximum test accuracy in software are shown in Table II. DS-CNN[†] model consists of eight depth-wise Separable (DWS) layers comprising depth-wise and point-wise layers with the input cochleagram of size 30×32 extracted from cascade of asymmetric resonators [5]. The global average pooling (GAP) layer reduces the input to the fully connected (FC) layer where the classification takes place. It is to be noted that the DS- CNN^{\dagger} model is much smaller in size as compared to the MobileNetV1[†] model which has 13 DWS layers sandwiched between CONV and FC layer. The input to the MobileNetV1[†] model is a pre-processed image of size 96×96 image derived from a 224×224 RGB image which is downsized and greyscaled as part of the pre-processing. It is also worthwhile to note that the pre-processing is being done offline and not at run-time.

TABLE II: Model statistics implemented on RAMAN.

Layer	$H_{in} \times W_{in} \times M$	$H_{out} \times W_{out} \times N$
CONV	$30 \times 32 \times 1$	$28 \times 30 \times 64$
DW	$28 \times 30 \times 64$	$28 \times 30 \times 64$
PW	$28 \times 30 \times 64$	$28 \times 30 \times 64$
DW	$28 \times 30 \times 64$	$14 \times 15 \times 64$
PW	$14 \times 15 \times 64$	$14 \times 15 \times 64$
DW	$14 \times 15 \times 64$	$7 \times 8 \times 64$
PW	$7 \times 8 \times 64$	$7 \times 8 \times 64$
DW	$7 \times 8 \times 64$	$4 \times 4 \times 64$
PW	$4 \times 4 \times 64$	$4 \times 4 \times 64$
$DW \times 4$	$4 \times 4 \times 64$	$4 \times 4 \times 64$
$PW \times 4$	$4 \times 4 \times 64$	$4 \times 4 \times 64$
GAP	$4 \times 4 \times 64$	$1 \times 1 \times 64$
FC	$1 \times 1 \times 64$	$1 \times 1 \times 12$
	(a) DS-CNN	1†

Layer	$H_{in} \times W_{in} \times M$	$H_{out} \times W_{out} \times N$
CONV	$96 \times 96 \times 1$	$47 \times 47 \times 16$
DW	$47 \times 47 \times 16$	$47 \times 47 \times 16$
PW	$47 \times 47 \times 16$	$47 \times 47 \times 16$
DW	$47 \times 47 \times 16$	$24 \times 24 \times 16$
PW	$24 \times 24 \times 16$	$24 \times 24 \times 32$
DW	$24 \times 24 \times 32$	$24 \times 24 \times 32$
PW	$24 \times 24 \times 32$	$24 \times 24 \times 32$
DW	$24 \times 24 \times 32$	$12 \times 12 \times 32$
PW	$12 \times 12 \times 32$	$12 \times 12 \times 64$
DW	$12 \times 12 \times 64$	$12 \times 12 \times 64$
PW	$12 \times 12 \times 64$	$12 \times 12 \times 64$
DW	$12 \times 12 \times 64$	$12 \times 12 \times 64$
PW	$12 \times 12 \times 64$	$12 \times 12 \times 128$
$DW \times 5$	$12 \times 12 \times 128$	$12 \times 12 \times 128$
$PW \times 5$	$12 \times 12 \times 128$	$12 \times 12 \times 128$
DW	$12 \times 12 \times 128$	$6 \times 6 \times 128$
PW	$6 \times 6 \times 128$	$6 \times 6 \times 256$
DW	$6 \times 6 \times 256$	$6 \times 6 \times 256$
PW	$6 \times 6 \times 256$	$6 \times 6 \times 256$
GAP	$6 \times 6 \times 256$	$1 \times 1 \times 256$
FC	$1 \times 1 \times 256$	$1 \times 1 \times 2$

(b) MobileNetV1[†]

TABLE I: Classes of the target applications

KWS Classes					
Class	Keyword	Class	Keyword		
0	Unknown	6	Left		
1	Silence	7	Right		
2	Yes	8	On		
3	No	9	Off		
4	Up	10	Stop		
5	Down	11	Go		

(a)	KW	S
· · · · /		

VW	VWW Classes				
Class	Status				
0	Person				
1	Not a person				
I Not a person					

(b) VWW

X. PERFORMANCE ANALYSIS

In this section, we analyze memory accesses throughout the hierarchy separately as reads and writes in both DS-CNN[†] and MobileNetV1[†] models. Also we try to analyze the reduction of reads and writes with and without IA sparsity, with and without parameter pruning. Additionally, we try to analyze the effects of IA sparsity and parameter pruning on MAC operations. To benchmark our results, we have taken 110 audio signatures and 110 images as inputs to average the operations (OPs) and memory accesses involved in inferring them. In our work, a read or write to the GLB-MEM or to the cache bank is considered to be a memory access.

FABLE III: Activation Global Memory Access in	KI	B
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	Activation Global				
DS-CNN [†]	Memory (in KB)				
	Read	Write			
Total CONV	0.96	53.76			
Total DW	128.64	75.904			
Total PW	75.904	75.904			
Total GAP	1.024	0.064			
Total FC	0.064	0.012			
Total	206.592	205.644			
(a) DS-CNN [†]					

	Activation Global				
MobileNetV1 [†]	Memory (in KB)				
	Read	Write			
Total CONV	9.216	35.344			
Total DW	245.792	192.016			
Total PW	334.864	219.664			
Total GAP	9.216	0.256			
Total FC	0.256	0.002			
Total	599.344	447.282			
(b) MobileNetV1 [†]					

(*)

DS-CNN^{\dagger} being a statiscally smaller model as compared to MobileNetV1^{\dagger}, the activation GLB-MEM reads and writes in Table IIIa are much lower than that shown in Table IIIb. It can also be observed that the depth-wise separable (DWS) layers constitute maximum activation GLB-MEM accesses (both reads and writes) which justfies our focus on optimising DWS layer dataflow and the hardware architecture to the maximum extent possible.

TABLE IV: Activation Cache Access in KB

Activation Cache Access (in KB)						
Read Write						
Without	With	Without With				
IA Sparsity IA Sparsity		IA Sparsity	IA Sparsity			
359.232	219.099	205.568	124.355			
(a) DS-CNN [†]						

Activation Cache Access (in KB)						
Read Write						
Without	Without With		With			
IA Sparsity	IA Sparsity	IA Sparsity	IA Sparsity			
978.848	538.343	590.128	323.36			
$(L) M_{-1} (1-N) (4) (1^{\dagger})$						

(b) MobileNetV1

The data shown in Table IV are the total cache accesses made for activations. The writes are $\approx 40\%$ less than reads which indicates extensive reuse of activations in the cache before being evicted out. $\approx 40 - 45\%$ reduction in accesses is seen when IA sparsity is exploited using ASE with RAP threshold set to zero, out of which the majority of the accesses happen in DWS layers itself.

TABLE V: Activation Cache accesses breakdown

	Activations Cache Access in KB					
Layer	With IA sparsity		Layer With IA sparsity With		Without	IA sparsity
	Read		Read	Write		
Total CONV	0.479	0.171	2.688	0.96		
Total DW	171.029	76.656	280.512	128.64		
Total PW	47.463	47.463	75.904	75.904		
Total GAP	0	0	0	0		
Total FC	0.128	0.064	0.128	0.064		
Total	219.099	124.355	359.232	205.568		
() DC CDD [†]						

(a) DS-CNN[†]

	Activations Cache Access in KB					
Layer	With IA	sparsity	sparsity Without			
	Read Write I		Read	Write		
Total CONV	9.852	6.708	13.536	9.216		
Total DW	355.661	143.822	630.192	245.792		
Total PW	172.574	172.574	334.864	334.864		
Total GAP	0	0	0	0		
Total FC	0.256	0.256	0.256	0.256		
Total	538.343	323.36	978.848	590.128		
			-			

(b) MobileNetV1[†]

Table V shows the breakdown of Table IV. Majority of the accesses are evidently done during the execution of DWS layers.

TABLE VI: Number of Operations in Million

#Operations (in Million)						
Weight Sparsity in	Without	With				
PW layer	IA sparsity	IA sparsity				
0%	12.052	7.099				
25%	9.623	5.581				
50%	7.194	4.062				
75%	4.765	2.543				
(a) DS-CNN [†]						

#Operations (in Million)						
Weight Sparsity in	Without	With				
PW layer	IA sparsity	IA sparsity				
0%	41.802	21.055				
25%	32.378	16.385				
50%	22.953	11.716				
75%	13.528	7.046				
(b) MobileNetV1 [†]						

Table VI shows the number of operations for both cases, with and without input sparsity. The baseline again would be a model without exploiting input and weight sparsity. We find a significant reduction of operations with IA sparsity when coupled with parameter pruning. We find that operations



Fig. 12: Weight Cache Access in KB

reduce by $\approx 54\%$ when the parameters are 25% pruned (12.05 Mil. vs 5.58 Mil.) whereas it further reduces by another $\approx 55\%$ when parameters are 75% pruned (5.58 Mil. vs 2.54 Mil.). It should be noted that even without IA sparsity, just parameter pruning also gives considerable reductions in operations. For example, operations reduce by 21% when compared to a 25% pruned model (9.62 Mil. vs 12.05 Mil.) and 61% when compared to a 75% pruned model (4.76 Mil. vs 12.05 Mil.). PW layers dominate other layers regarding the number of operations and contribute to nearly 90%

Fig. 12 depicts the cache accesses (reads and writes) involved in the parameter space. According to the dataflow described in the main document, cache bank is used only to store PW layer parameters. Hence, the plot are accesses related to PW layers in the model. The reads for any given pruning percentage is much higher than writes, which implies that there is considerable reuse of weights present in the cache. Also, the reads and writes reduce as the pruning percentage increases.

Fig. 13 depicts the effect of ASE on the memory accesses in parameter reads. The parameters are not read from the cache when all the elements of a column are zero (for instance columns 2 and 3 in Fig. 14). This reduces the parameter reads to a great extent leading to considerable latency and power saving. This plot shows the effectiveness of ASE in not only exploiting input activation sparsity but also reducing the parameter reads to a great extent.

The memory and power breakdown of the RAMAN architecture is shown in Fig.15 and Fig.16 considering 75% weight pruning in the PW layers. The parameter memory (54% util.) dominates the activations (26% util.) for the MobileNetV1[†] model, whereas the activation memory (46% util.) dominates the parameters (25% util.) for the DS-CNN[†] model. The cache and Instruction Memory+ASE buffers account for 16 - 23% and 4 - 6%, respectively. The power breakdown is as follows; logic+clock account for 80%, and the memory+DSP account for the remaining 20%.

A. Model-wise Analysis:

The number of operations and memory accesses of DS-CNN^{\dagger} and MobileNetV1^{\dagger} vary significantly based on the sparsity of the given input. Also because the model statistics (as shown in Table II) vary significantly between both the



Fig. 13: Weight Cache Reads in KB



Fig. 14: ASE illustration for the PW layer.

models, it is important to analyze RAMAN's performance for both the models separately.

1) DS-CNN^{\dagger}: Table VII summarizes the performance of RAMAN for the DS-CNN^{\dagger} model, which consists of eight

DWS layers with 50% weight pruning in the PW layers. It is observed that the pre-processed audio input (cochleagram) fed to the CONV layer is highly sparse (82.2%). The activation cache accesses total just 0.651KB (0.479KB reads and 0.171KB writes), as the cache memory doesn't store zeros. These accesses translate to 0.172M OPs which is \approx 80% lower when IA Sparsity is not exploited. CONV employs the DW dataflow and doesn't require parameter cache accesses; thus, the parameters are directly accessed from the GLB-MEM.

DWS layers follow the CONV layer. From Table VII, it is evident that activation cache access is 247.684 KB, which is $\approx 21\%$ higher than the activation GLB-MEM accesses. With an average IA sparsity of 22.7%, there is a reduction of $\approx 38\%$ (0.849 Mil.) in the operations when IA Sparsity is exploited.

The PW layer employs the RD dataflow, as discussed in the main document. The parameter cache access (888.044) dominates the GLB-MEM accesses (27.648KB), leading to effective temporal cache reuse of about 32x. There is a 3x reduction in operations with IA Sparsity (37.5%) and 50% weight pruning.

The global average pooling (GAP) layer reduces each input



Fig. 15: Memory breakdown of RAMAN for (a) MobileNetV1^{\dagger} model and (b) DS-CNN^{\dagger} model for 75% weight pruning in the PW layers.



Fig. 16: Power breakdown of RAMAN for (a) MobileNetV1^{\dagger} model and (b) DS-CNN^{\dagger} model for 75% weight pruning in the PW layers.

TABLE VII: Performance Breakdown of DS-CNN^{\dagger} model with 8 DWS layers. The RAP threshold was set to zero and the parameter pruning in the PW layers was set to 50%

Layer	Activation GLB-MEM accesses (KB)	Parameter GLB-MEM accesses (KB)	Activation Cache accesses (KB)	Parameter Cache accesses (KB)	OPs (in Mil.)	Num. of Active PEs	Avg. IA Sparsity (%)
CONV	54.72	0.96	0.651	0	0.172	11 (91.67%)	82.2
DW	204.544	7.68	247.684	0	0.849	11 (91.67%)	22.7
PW	151.808	27.648	94.927	888.044	3.038	12 (100%)	37.5
Pooling	1.088	0	0	0	0.001	-	72.5
FC	0.076	1.056	0.192	0	0.002	12 (100%)	66.8
TOTAL	412.236	37.344	343.454	888.044	4.062	-	28.6

TABLE VIII: Performance Breakdown of MobileNetV1[†] model which has 13 DWS layers. The RAP threshold was set to zero and the parameter pruning in the PW layers was set to 50%

Layer	Activation GLB-MEM accesses (KB)	Parameter GLB-MEM accesses (KB)	Activation Cache accesses (KB)	Parameter Cache accesses (KB)	OPs (in Mil.)	Num. of Active PEs	Avg. IA Sparsity (%)
CONV	44.56	0.240	16.561	0	0.463	11 (91.67%)	27.2
DW	437.808	18.720	499.483	0	1.904	11 (91.67%)	35.1
PW	554.528	157.536	345.147	3620.764	9.339	12 (100%)	44.9
Pooling	9.472	0	0	0	0.009	-	59.8
FC	0.258	0.8	0.512	0	0.001	12 (100%)	7.1
TOTAL	1046.626	177.296	861.704	3620.764	11.716	-	39.5

channel to a single value. In RAMAN, during the execution of the GAP layer, the entire PE array is gated to reduce dynamic power consumption, and the entire execution takes place in the PPM. GAP constitutes a tiny percentage of operations and memory accesses.

The FC layer leverages IA reuse; hence, we observe that the activation cache accesses are $\approx 2.5 \times$ more than the activation GLB-MEM accesses. The parameters are directly accessed from the GLB-MEM, bypassing the cache due to no reuse.

A further $\approx 10\%$ reduction in IA cache access and $\approx 13\%$ reduction parameter cache reads were observed with run-time activation pruning with the threshold value of 30.

2) *MobileNetV1*[†]: MobileNetV1[†] model has 13 DWS layers which account for higher memory access and operations as indicated by Table VIII in comparison with the DS-CNN[†] model. The estimates shown are for 50% weight pruning and leveraging IA sparsity. The DW and the PW layers dominate the GLB-MEM activation and parameter accesses, and the

same trend is observed in the cache access. The weights are stored in the cache only in the PW dataflow leading to a temporal reuse of about 23x. Run-time activation pruning with the threshold value of 40 led to an additional $\approx 8\%$ decrease in IA cache access and $\approx 21\%$ reduction in parameter cache reads.

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