A Miniature Wireless Silicon-on-Insulator Image Sensor for Brain Fluorescence Imaging

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***Abstract*— Optical recording of genetically encoded calcium indicator (GECI) allows neuroscientists to study the activity of genetically labeled neuron populations, but our current tools lack the resolution, stability and are often too invasive. Here we present the design concepts, prototypes, and preliminary measurement results of a super-miniaturized wireless image sensor built using a $32\mathrm{nm}$ Silicon-on-Insulator process. SOI process is optimal for wireless applications, and we can further thin the substrate to reduce overall device thickness to $\sim 25\mu\mathrm{m}$ and operate the pixels using back-side illumination. The proposed device is $300\mu\mathrm{m} \times 300\mu\mathrm{m}$. Our prototype is built on a $3 \times 3\mathrm{mm}$ die.**

I. Introduction

Recording genetically selective neural activity in freely behaving animals is crucial for understanding complex neural mechanisms. Unfortunately, our tools lack resolution, stability, specificity and are often too invasive. Commonly used multi-electrode recording lacks the selectively to unambiguously track well-defined populations of cells over long time periods. Genetically encoded calcium indicators (GECIs) provide the means for single-cell level genetically selective measurements, but our imaging tools suffer from the tradeoff between resolution and invasiveness: fiber photometry provides imaging depth, minimizes tissue damage but is limited by resolution [1]. Miniature single-photon endoscopy can record simultaneous activity across many cells, but targeting deeper brain regions requires invasive insertion of lens and/or aspiration of brain tissues [2].

There have been recent work to minimize the camera size so they can be inserted directly into the brain with minimal damage: Ohta et al. proposed the idea to use implantable microimaging sensors to record GECI activity in the brain [3]. Adams et al. demonstrated a flat lensless fluorescence camera by placing a patterned mask close to the image sensor, achieving overall system thickness of $1mm$ [4]. Shin et al. coupled a miniature mask to the end of a fiber bundle, which is then inserted into the brain tissue as an endoscope without additional microlens [5]. The fiber bundle can target deep brain regions, but with a diameter of $400\mu m$, its damage to the brain tissue can not be ignored. To further reduce the system size and thickness, Choi et al. described a system with thin shanks filled with single-photon avalanche photodiodes (SPADs) that can record fluorescent activity of neurons over the axis of insertion [6]. Using post processing to remove extra silicon substrate, the insertion shank's thickness is reduced to around $40\mu m$, but further thinning would cause damage to the photodiode inside the bulk silicon.

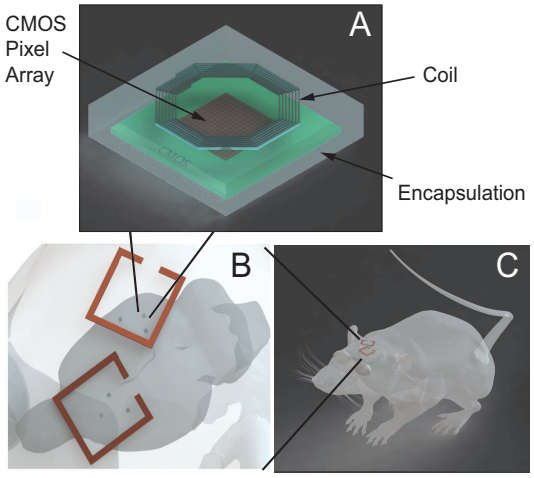

Fig. 1. Conceptual drawings of the proposed device. **A**, The proposed wireless image sensor. **B** and **C**, the proposed device implanted in the brain of the rat with a power delivering coil placed above the skull.

Here we explore an idea to push this limitation even further to design ==a small, thin, wireless powered image sensor that can be embedded within the brain tissue. Previous works on photodiodes designed using silicon-on-insulator (SOI) processes offer inspirations: The lateral PIN photodiodes is much thinner compared to conventional photodiodes built using bulk silicon processes [7][8]. Thus, we can further thin the substrate to reach below $40\mu m$ of device thickness — less than the diameter of a human hair. Another advantage of SOI process is that the buried oxide layer is transparent to light. With device thinning, we can operate the image sensor using back-side as well as front-side illumination to enhance quantum efficiency. Using back-side illumination would give us the freedom to pattern top metal layers. In a wireless device, this transfers to area-saving design by placing RF inductor and capacitors directly on top of the photodiodes. Finally, SOI processes have higher power transmission efficiency compared to bulk CMOS processes, which makes it an optimal choice for low power wireless applications, like our proposed device.

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The conceptual drawing of the proposed system is shown in Fig.1A. RF power and data transmission coil and capacitors are placed directly on top of the pixel array, which consists of PIN photodiodes to sense fluorescent signal through back-side. The entire encapsulated chip would measure only $300\mu m \times 300\mu m$ with thickness of 25 μm, and is designed such that multiple devices can be injected directly into the brain using a small needle (<24 Gauge). A power transmission coil is on top of the scalp to inductively deliver power to these small devices, shown in Fig.1B and C. We prototyped parts of this system using a $32nm$ SOI process, which include power harvesting circuits, PIN photodiodes, as well as post-processing that reduce the silicon thickness at the backside to $< 10\mu m$. Our prototype devices presented in this work is $3\times3mm$ in size. In the following sections, we present the design, fabrication and preliminary measurement results.

II. Power Harvesting

For wireless implantable micro-devices, the size of the device is limited by the LC resonator design trade-offs: Power transmission efficiency decreases with LC resonator frequency, which is inversely proportional to the value/physical size of inductor and capacitors. We have found that using the $32nm$ SOI process, a resonator frequency of $270MHz$ offers the best design trade-offs, which corresponds to a resonator using a $157nH$ inductor and a $2.2pF$ capacitor. The power harvesting circuit is shown in Fig. 2. To reduce size, the LC resonator is made from a $300\mu m \times 300\mu m$ inductor with carefully tuned parasitic capacitance. The parasitic capacitance include the gate capacitance and the contribution from the on-chip capacitors of the charge-pump rectifier.

The circuit encircled in red is the charge pump rectifier which includes two rectifier stages that are connected in series with the RF signal being fed into later stages through coupling capacitors. The rectifier is a cross-connected bridge rectifier that uses thick oxide low-Vth transistors. This allows us to operate up to an unregulated voltage of 2.1V and also reduces the drop across the diodes and the input voltage swing needed to turn-on the diodes. === The circuit encircled in purple is the low-dropout regulator (LDO). To improve the LDO stability and decrease the large output capacitor, a compensation capacitor is added to connect the output of the op-amp to the regulator's output. When generating an unregulated voltage of 1.1V, the power conversion efficiency of the charge pump rectifier has been simulated when drawing 1mA using a resistive load and is found to be 80% for a frequency of $270MHz$. The LDO consumes $25\mu W$ for a regulated voltage of $1V$.

A highly optimized transmitter coil designed following the methodology described in [9] is placed $4mm$ above the CMOS device to transmit power wirelessly. The power transfer efficiency was measured to be 0.002% when the power delivered to the load is $1mW$.

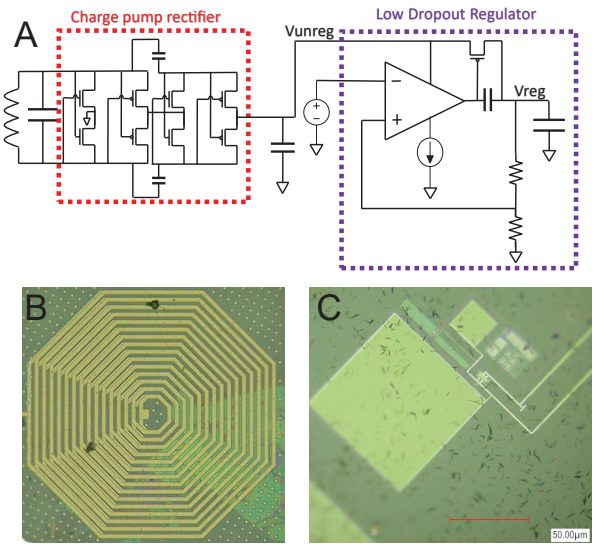

Fig. 2. The schematic and micrograph the power harvesting circuits. **A**, Circuit schematic. **B** and **C**, Micrographs of the inductor and the rest of circuit respectively.

III. Pixel Array

The pixel array is the core of this system, and its design and data rate must be carefully regulated to minimize power consumption — arguably one of the most important design specifications. Low power design is important because a super-miniaturized system, like the one proposed here, has poor heat dissipation efficiency due to small surface area. When placed at close proximity to the brain tissue, unconstrained power dissipation rises tissue temperature locally and may cause undesirable physiological effects.

In a wireless implantable device, a majority of the power is allocated to the data transmission block, whose power is directly proportional to the data rate for a fixed transmission range and bit rate error (BER) specificition. To reduce sampling and transmission data rate, we designed the pixel array to compressively sample the scene using pixel-wise exposure (PCE) imaging [10][11][12][13]. By controlling each pixel's exposures, PCE allows pixel level implementation of spatio-temporal compressive sensing, that enables sub-Nyquist sampling and reconstruction of videos — a sparse signal. Here we briefly summarize the mechanism of PCE and refer the readers to a detailed discussion on PCE imaging in our previous publication [10].

Pixel-wise coded exposure: Fig.3 illustrates the mechanism of the PCE pixels. In a CMOS active pixel sensor (APS), an extra exposure control transistor EX is inserted between the photodiode and the rest of the readout structure. Shown in Fig.3, when EX is high, this pixel is the same as a conventional APS where RST pulses high to empty charges accumulated at the photodiode (PD). RST then drop low to allow photon induced electrons to integrate at the PD parasitic capacitor. But when EX is low, the PD is separated from the rest of the readout. The RST pulse cannot reset the

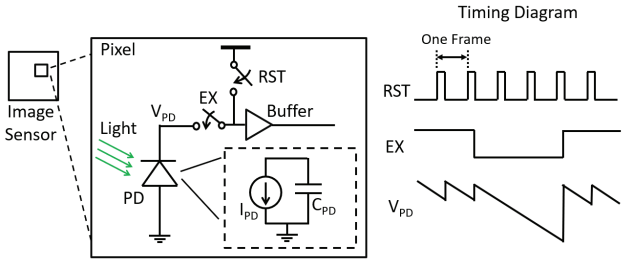

Fig. 3. Design and timing diagram of illustrating pixel-level exposure control in PCE imaging

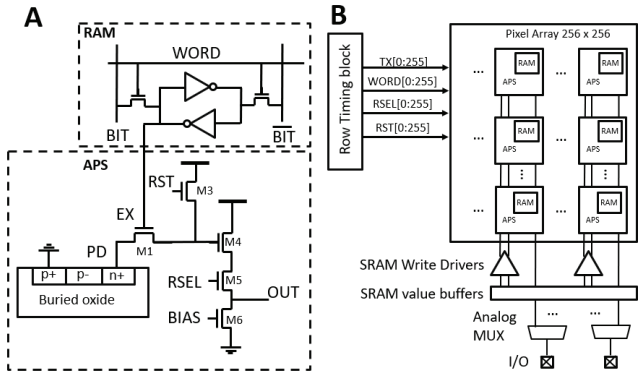

Fig. 4. Schematics of a PCE pixel (A) and the block diagram of the pixel array (B)

charge at PD, and its exposure is prolonged. By controlling the timing of EX transistor, we can control the precise duration of each pixel's exposure. We have shown that using pseudorandom exposure patterns, we can compress a 30 FPS video into $<$ 3 FPS equivalent sample corresponding to compression rate of $> 10\times$ [10]. We have also shown that in a ultra-wide band wireless system, $10\times$ reduction of data rate can reduce transmission power by $10dB$ [14].

Fig. 4 shows the circuit implementation of the PCE pixel and the array. A 1-bit memory in pixel memory is used to control the timing of the EX transistor. The RST and RSEL are reset and row select signals respectively, similar to a 3T APS used in rolling shutter readout. The prototype pixel array consists 256×256 pixels, with SRAM drivers to write the in-pixel memory. For the prototype, we simply multiplexed the output of pixel columns to analog output pins to directly measure the pixel response. The image sensor array consumes around $300\mu W$ at VDD of $1.4V$.

PIN photodiode: The photodiode in our design is constructed using lateral P-I-N structure composed of a lightly doped P-type channel between heavily doped N-type and P-type diffusions, shown in Fig.4(A). The pixel pitch is $4\mu m$, shown in Fig. 5. Compared to diodes built using PN junction of a conventional deep substrate, the lateral diodes sacrifice quantum efficiency for overall thinner substrate thickness. PIN photodiodes have been built using Silicon-on-Sapphire processes (SOS)[7][8]. The advantage of SOS over SOI is the sapphire's transparency allows for high efficiency back-side illuminated imaging, whereas SOI the buried oxide is placed on top of a thick handle substrate that is not transparent to visible light. In the next subsection, we describe our post-processing methods to remove this thick substrate to allow for back-sided illumination.

A. Post-processing

Since the on-chip coil is above the image sensor, front-side illumination will not be effective as most photons will be blocked. Therefore a process flow was developed and implemented to allow for back-side illumination. As silicon is opaque, a SOI process was chosen for this work in order to allow for the complete or partial removal of the bulk silicon.

The post-processing process works directly with dies instead of wafers. After receiving the SOI dies from the foundry, the dies are thinned down to approximately $30\mu m$

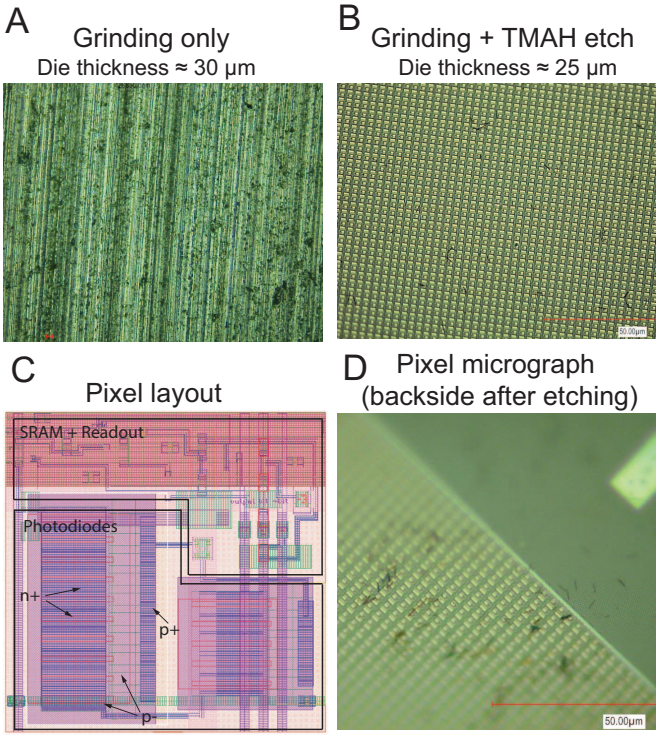

Fig. 5. Micrograph of the back-side with thinning: A, with only grinding. B, with grinding and TMAH etching. C, Layout of the pixel, D, Pixel micrograph from the backside after etching.

overall thickness using a mechanical polishing system. Grinding techniques typically do not offer the resolution needed to completely remove the silicon below the 145nm thick buried oxide. Therefore, the silicon is removed by wet-etching using tetramethylammonium hydroxide (TMAH) while using the buried oxide layer as an etch stop. Fig. 5 illustrates the view of the die during these processes. TMAH has good selectivity and is CMOS compatible as it has no mobile K+ contamination (unlike KOH). However, the downside is that TMAH etches the aluminum pads, which are needed to test the functionally of the ASIC chip before further post-processing. Fortunately, a solution to this problem was proposed in [15] and involves dissolving an

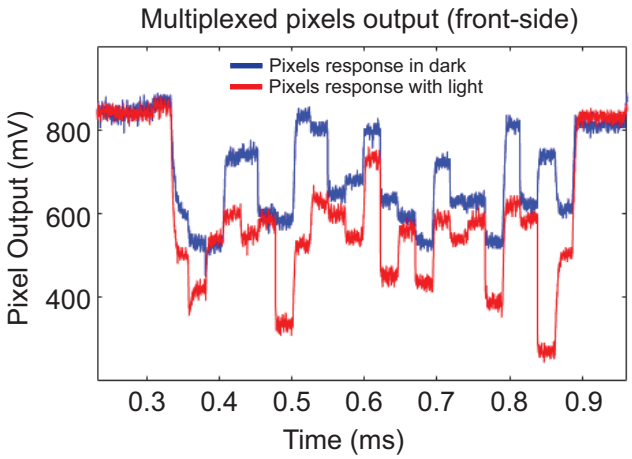

Fig. 6. Time-multiplexed pixel output under front-side illumination. Each step is a pixel reading at the in-pixel buffer during a 20 pixel time-multiplexed scan. Lower voltage reading corresponds to more charge integrated at the pixel.

appropriate amount of silicon in TMAH. The silicon powder forms aluminosilicates on Al which serves as a passivation layer. With the carrier substrate removed the remaining system is completely encapsulated in silicon dioxide, which has a low water vapor permeability. Therefore, after dicing the ASIC to get rid of the pads, the device can already be utilized for acute experiments without any additional encapsulating coatings.

We first test the performance of photodiode array by shining light directly onto the front-side. Fig. 6 illustrates the time-multiplexed results of 20 columns of pixels in dark and with light. Despite large non-uniformity in pixel response, which can be corrected later during non-uniformity correction, this shows the operation of the lateral PIN photodiodes. We are currently working on comparing the back-side illumination results with the front-side illumination, but we had encountered difficulties with wirebonding, due to weakened mechanical structure of the larger $3mm \times 3mm$ prototype chip, especially for the thinnest die with thickness of $< 30\mu m$. We have developed methods to handle these dies to complete this test setup, and expect to have good pixel response from back-illumination.

IV. Discussion and Conclusion

The presented work is to be seen as the initial steps taken in achieving a prototype aiming at taking fluorescent images distributed across the brain. There are still numerous obstacles to overcome for the use of these devices in animal studies. One of them is the fluorescent excitation light source. What is the most efficient and minimally invasive method to couple the excitation light efficiently to the tissue? Possible solutions are light delivering fibers, implantable micro-LEDs [16], and the possibility of attaching an excitation LED on the recording device. These solutions all have clear benefits and disadvantages, and finding the optimal method is still an active area of research

To summarize, we have demonstrated the feasibility, design concepts and preliminary measurement results of the micro-imaging device. We are currently working on completing the test of the back-side illumination using the PIN photodiodes, and a standalone chip integrating the parts described in this paper.

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